The SAD-4096 is a general purpose 4096-bucket (2048-sample) n-channel bucket-brigade audio delay line useful in applications where relatively long delay is desired, coupled with high performance. The signal is sampled at the clock rate, but the samples retain their analog values. Simple filtering applied at the output smooths the stairstep of samples to recover the analog wave form.

The delay is controlled by the clock frequency according to the relation $T_D = 2048/f_c$, so that a clock or sample rate of 40 KHz, for example, the delay is 51.2 milliseconds.

Key Features

- 2048 samples of audio signal delay
- Wide dynamic range: S/N 70 db (unweighted)
- Clock-Controlled Variable delay
- Sample rates from 8 KHz to 1 MHz
- Delays from 2 msec to 250 msec
- On-chip buffers provide full-wave output

Typical Applications

- Reverberation effects
- Sound effects
- Data buffering
- Speech scramblers

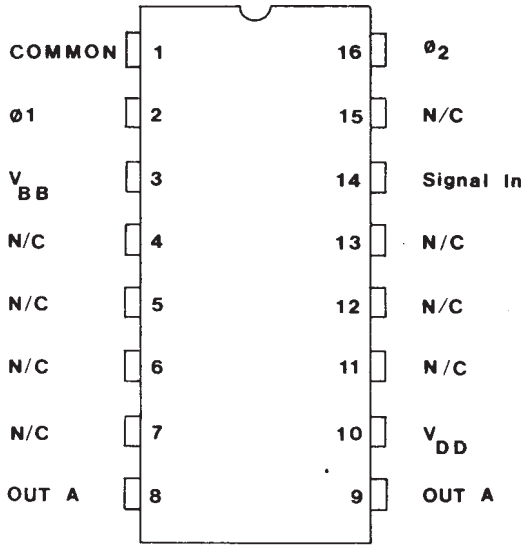

Figure 1. Pin Configuration for SAD-4096 18317

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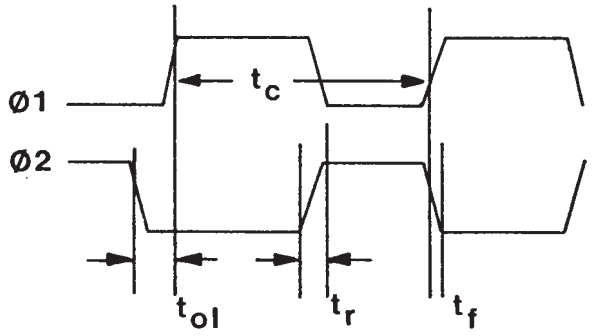
Absolute Maximun Ratings

Voltage on any pin to common (pin 1)	-0.5 to +18 volts dc or peak
Output Current	5 milliamperes
Temperature (operating)	0^{o} to 70^{o} C
Temperature (storage)	-55^{o} to 125^{o} C

Note: Long delays are limited by leakage to approximately o.25 second, at 25^{o} C at a clock rate of 8 KHz. At 70^{o}C, the minimum sample rate rises to more than 250 KHz.

Drive and Voltage Requirements

Normal voltage levels and linits are given in the specifications, Table I. The clock inputs are normally complementary square waves. The timing relationships are noncritical, so long as the crossing level is below the top quarter of the wave.



	Max	Typ	Min	Units
t_{ol}	$\frac{t_c}{2} - 50$	50	0	nsec
t_r		50	10	nsec
t_f		50	10	nsec

Figure 2. SAD-4096 Clock Timing Requirements

TABLE I

SAD-4096 Electrical Specifications (25°C)

Symbol	Function	Min	Typical	Max	Units
V_{DD}	Output Supply	8	12-15	18	Volts dc
V_{BB}	CTD Interstage Bias Voltage	8	$V_{\emptyset H}$-1	12	Volts dc
$V_{\emptyset 1H}$, $V_{\emptyset 2H}$,	CTD Clock Amplitude	-0.3	0	0.5	Volts p
$V_{\emptyset_1 H}$, $V_{\emptyset_2 H}$,		8 (1)	12-15	18	Volts p
V_{IB}	Input Bias	0.3	3 (2)	6	Volts dc
Vin	(V_{bb} = 11.5 volts)		2		Volts p-p
C$\emptyset$	Clock Line Capacitance		1000		pf
C_{in}	Input Capacitance			2	pf
f_c	Clock or sample rate	8	100	2000	KHz

Footnotes for Table I

(1) The device is operable to clock and supply voltages as low as 5 volts, but at substantially reduced signal levels.

(2) Input bias is dependent on the particular values of V_{BB}, $V_{\emptyset}$ and V_{DD}, so that adjustment provision should be made to fit the circumstances used.

(3) WARNING: Observe MOS Handling and Operating Procedures. Maximum rated supply voltages must not be exceeded. Use decoupling networks to suppress power supply turn on/off transients, ripple and switching transients. Do not apply independently powered or AC coupled signals or clocks to the chip with power off as this will forward bias the substrate. Damage may result if external protection precautions are not taken.

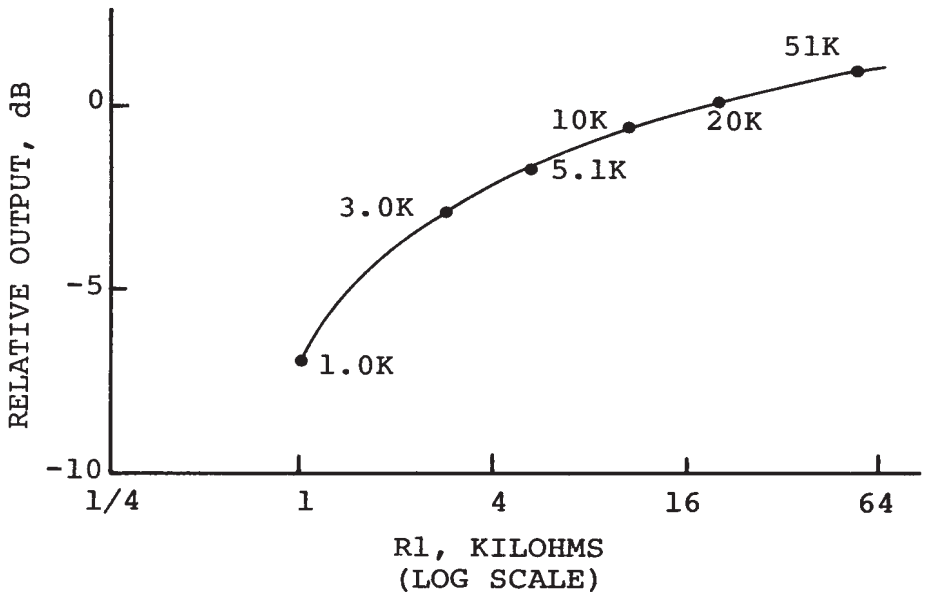


Figure 3. Effect of Load Impedance on Signal Output Level.

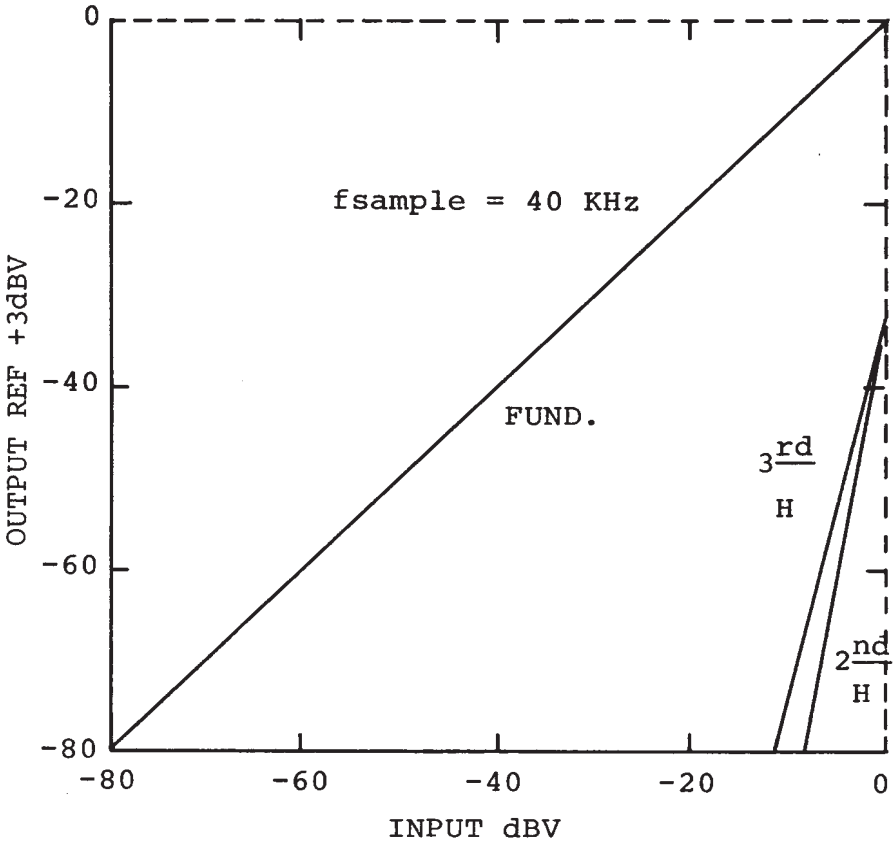


Figure 4. Signal and Harmonic Output Levels versus Input Level.

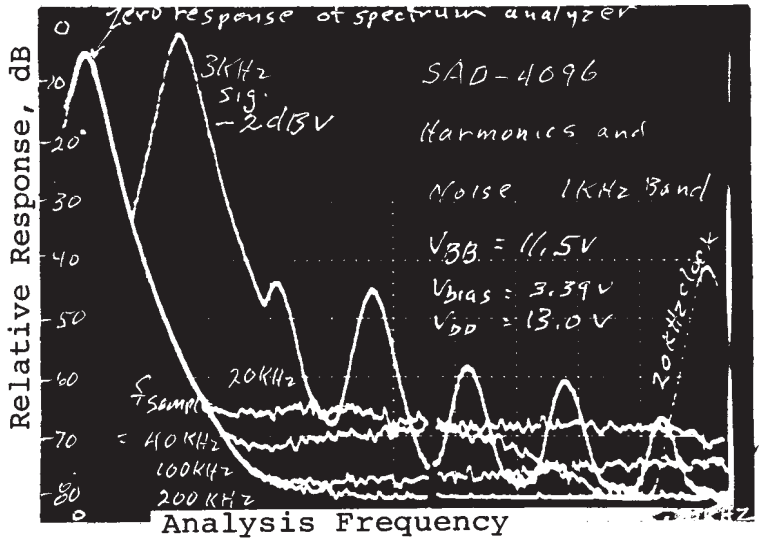


Figure 5. Spectrum Analyzer Response Showing a 3 KHz Signal and Four Traces of Noise Background at Sample Rates of 20, 40, 100 and 200 Kilohertz.

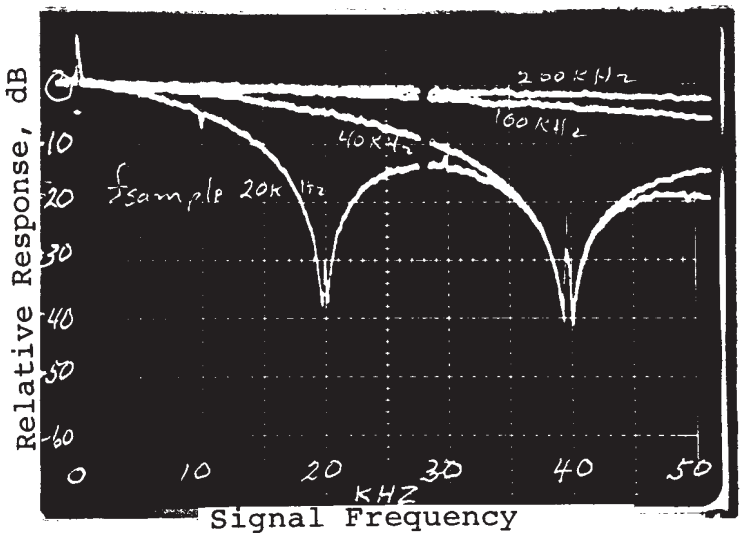
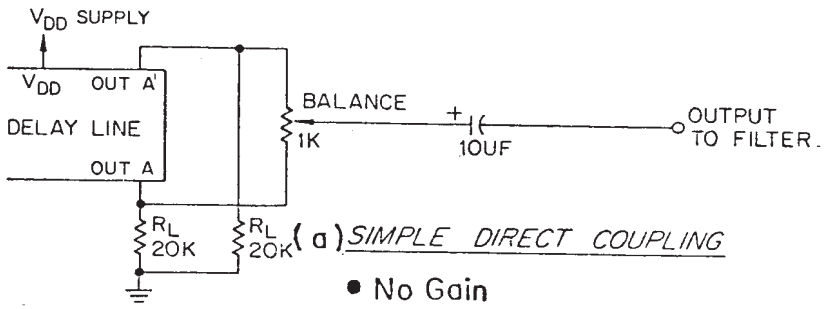


Figure 6. Frequency Response, with Output Filter, of SAD-4096 at Various Clock Rates.

Note:
Due to the $\frac{\sin x}{x}$ sampling, the response is down 3.92 db at the Nyquist frequency.

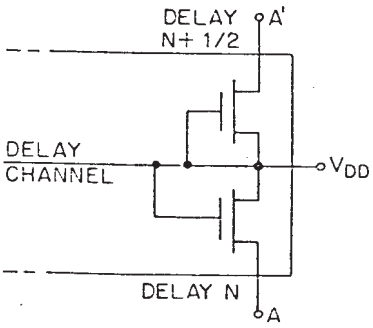
Figure 8. *SIMPLE OUTPUT CIRCUITS*

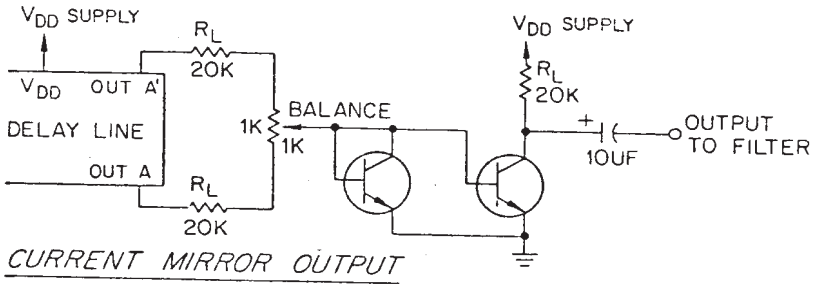


a) *SIMPLE DIRECT COUPLING*

- No Gain
- High Zout

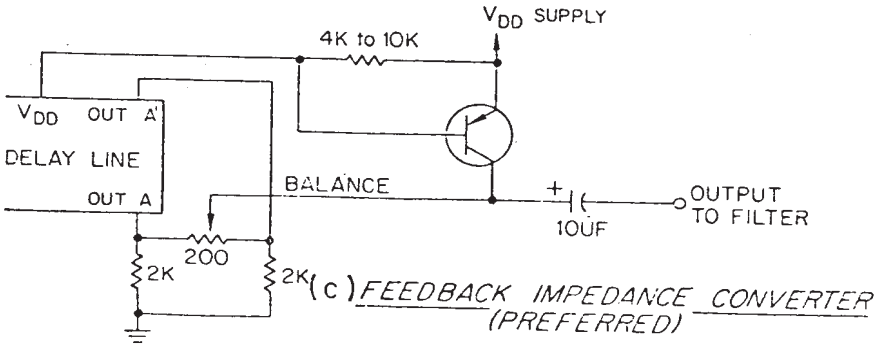
OUTPUT CIRCUIT OF DELAY LINE





b) *CURRENT MIRROR OUTPUT*

- Good Summer
- Relatively low Zout
- Limited gain



c) *FEEDBACK IMPEDANCE CONVERTER (PREFERRED)*

- Good frequency response
- Low Zout
- Simple circuit

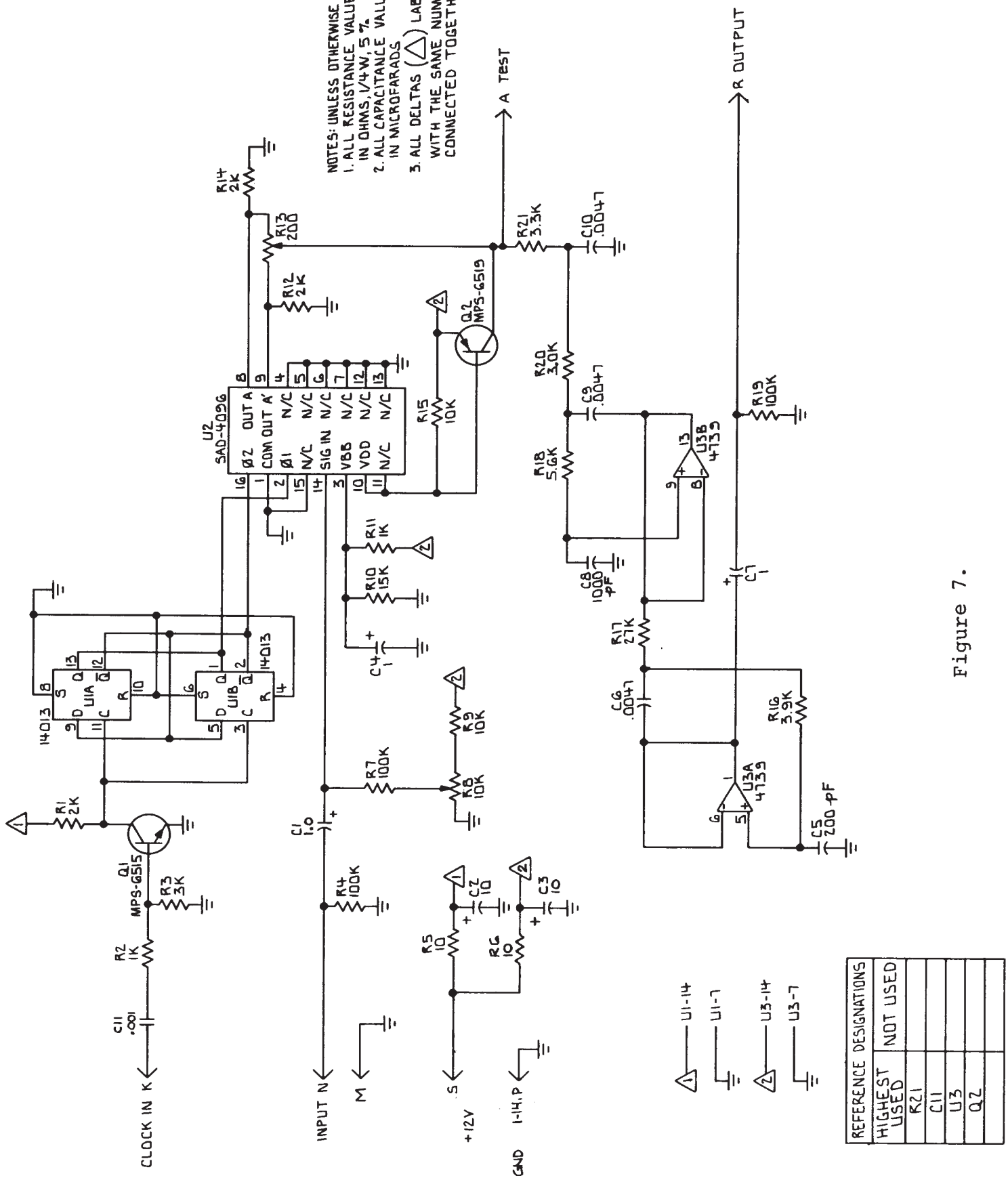


Figure 7.