6. Functional description

Table 3. Function table[1]

Inputs				Function
STCP	SHCP	$\overline{PL}$	$\overline{MR}$	
↑	X	X	X	data loaded to input latches
↑	X	L	H	data loaded from inputs to shift register
no clock edge	X	L	H	data transferred from input flip-flops to shift register
X	X	L	L	invalid logic, state of shift register is indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked Qn = Qn−1, Q0 = DS

[1] H = HIGH voltage level.
L = LOW voltage level.
X = don't care.
↑ = positive-going transition.

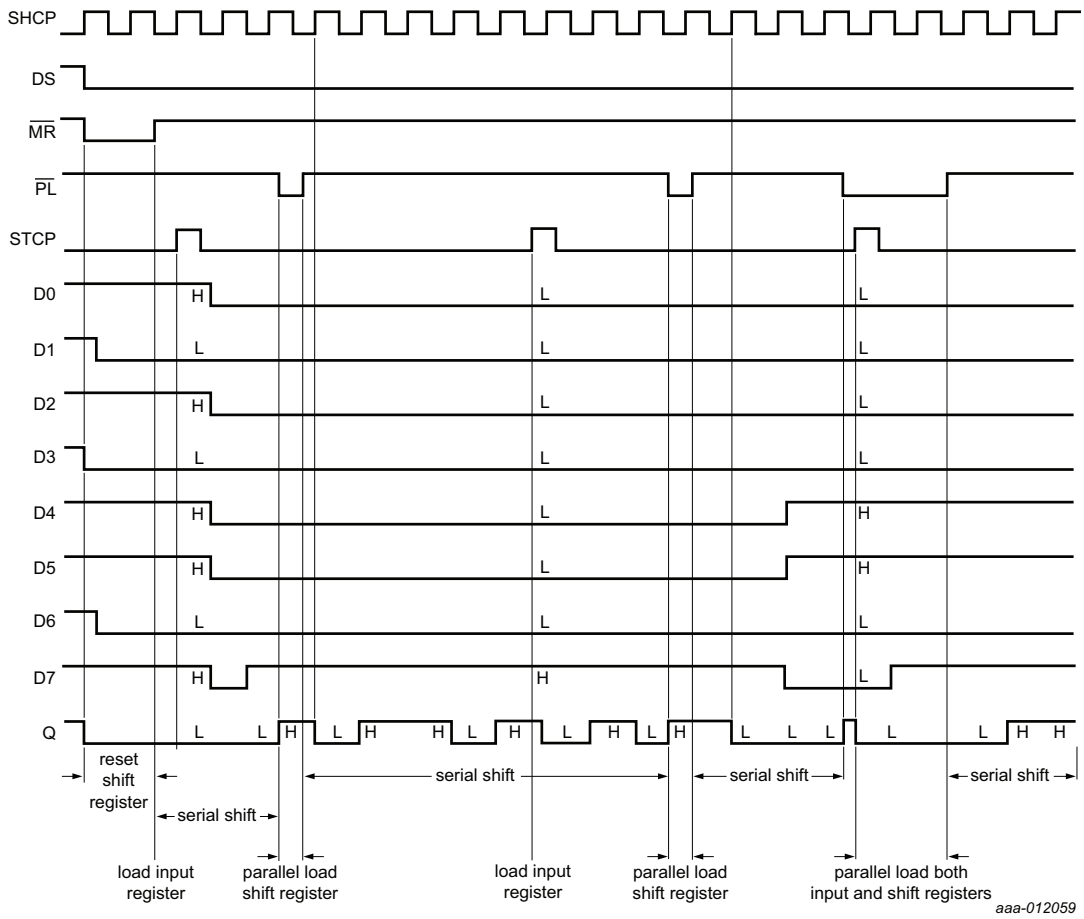

Fig 6. Timing diagram