

Silicon PNP Power Transistors

2SB407

DESCRIPTION

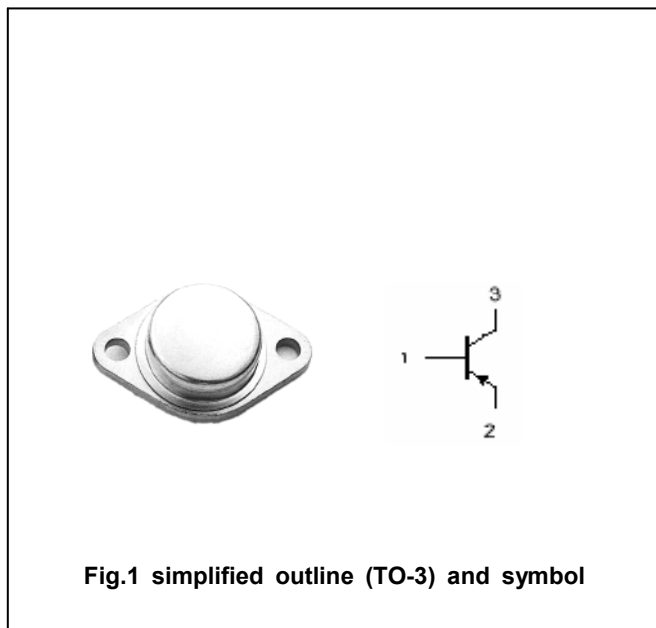
- With TO-3 package
- Low collector saturation voltage
- Wide area of safe operation

APPLICATIONS

- For power amplifier applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

**Absolute maximum ratings(Ta=□)**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-30	V
V_{CEO}	Collector-emitter voltage	Open base	-30	V
V_{EBO}	Emitter-base voltage	Open collector	-10	V
I_C	Collector current		-7	A
P_C	Collector power dissipation	$T_C=25^\circ$	30	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-10mA ; I _B =0	-30			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =-1mA ; I _E =0	-30			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =-1mA ; I _C =0	-10			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-6A ; I _B =-0.6A			-1.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-6A ; I _B =-0.6A			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-30V ; I _E =0			-10	μA
I _{EBO}	Emitter cut-off current	V _{EB} =-10V ; I _C =0			-10	μA
h _{FE}	DC current gain	I _C =-1A ; V _{CE} =-1.5V	80			

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PACKAGE OUTLINE



Fig.2 outline dimensions (unindicated tolerance:±0.1mm)