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B&K Model 282

DIGITAL MULTIMETER

DYNASCAN CORPORATION · Service Department
2815 W. Irving Park Road · Chicago, Illinois · 60618

SERVICE MANUAL

FOR

MODEL 282 3-1/2 DIGIT MULTIMETER

INDEX

1. CIRCUIT DESCRIPTION AND THEORY OF OPERATION

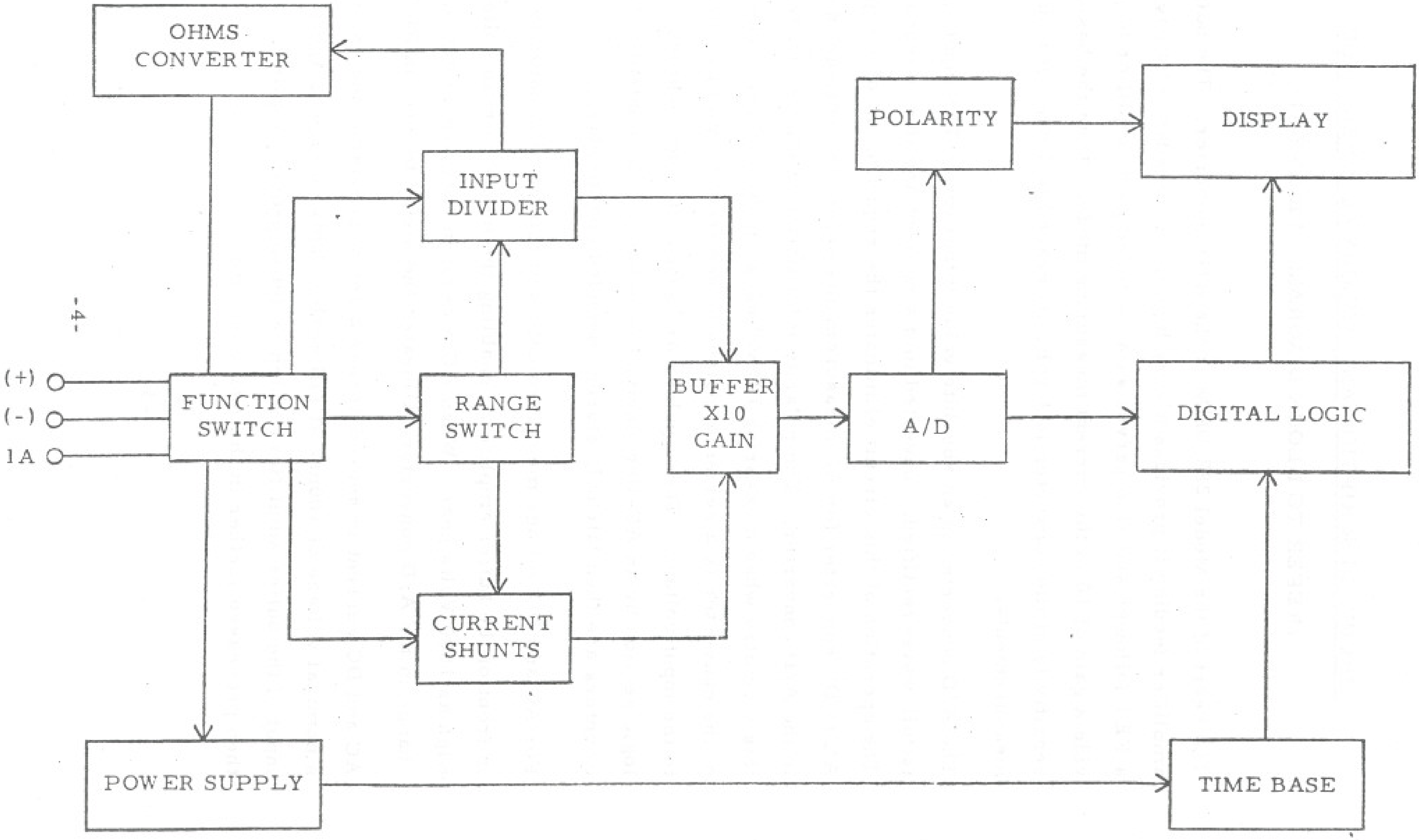
(REFER TO BLOCK DIAGRAM - FIGURE 1)

The heart of the Model 282 DMM is the A/D converter. The buffer amplifier feeding it provides a very high input impedance by use of a FET follower and also serves as a switched gain amplifier to provide a gain of 10 in the current measuring mode. Thus the basic sensitivity of the converter is 1 Volt, increased to 100mV for current measurements.

The A/D converter is an absolute value integrator. The input voltage is full-wave-rectified, converted into a current and then integrated. The operation of this circuit eliminates the requirement of a separate AC to DC converter for AC measurements before the voltage is applied to the A/D converter. The polarity information is also extracted from this circuitry when measuring DC voltages or DC current. The output of the converter is a series of pulses whose frequency is proportional to the input voltage. These pulses are gated into the counters of the logic section by an AC-line-derived time base. The contents of the counters are then latched, stored, decoded and displayed.

For AC and DC voltage measurements a precision attenuator is placed in front of the buffer amplifier, enabling the meter to read voltages as high as 1500 Volts peak. When AC measurements are selected, a gain change in the A/D converter calibrates the meter to read in RMS units.

AC and DC current is sensed across a set of precision shunts, developing a nominal voltage of 100mV at full scale. This voltage is applied to the input of the buffer amplifier, which is set to provide a gain of 10, and then processed further in the A/D converter.



MODEL 282 BLOCK DIAGRAM, FIGURE 1

For resistance measurements, a constant current source is connected to the input, developing a voltage drop across the unknown resistor that is proportional to its value.

A. VOLTAGE ATTENUATORS AND CURRENT SHUNTS

The input attenuators used in the voltage measuring mode consists of a compensated resistive divider string made up of four precision resistors: R1, R2, R3 and the series combination of R4, R5 and R6. The junctions of R4, R5 and R5, R6 are used in the OHMS mode only and do not affect the voltage measuring mode. R1 is not explicitly compensated since there is sufficient parasitic capacitance across it. Because the input divider is never disconnected for voltage measurements, the input impedance is a constant 10MΩ on all ranges. If the ACV function is selected, C17 serves to remove any DC voltage component from the signal to be measured.

For current measurements, resistors R7, R8, R9 and R10 are connected in series and form a precision shunt that drops a nominal 100mV for the selected range. Antiparallel diodes D10 and D11 limit the voltage across the shunt resistors to a safe value and prevent burn-out. For excessive input currents on the 1, 10 and 100mA range, fuse F1 (on rear panel) will blow out. Note that R10 is not protected by D10 or D11 and that it can only be accessed by the 1A front jack.

B. INPUT BUFFER AND AMPLIFIER

After passing thru the FUNCTION switch S2 and RANGE switch S1, the input signal appears at S2, contact 12. If S2 is in the DCV or DCA position the input filter consisting of R11 and C16 is switched in front of the input buffer by contact closure of terminal 8 and 9 on S2A. The input signal appears now at the gate of dual FET Q1. Q1 together with Q12 form a differential source follower. The constant current source made up of D9, R39 and Q12 draws a nominal 200µA thru each FET. Thus approximately 2 volts drop across R12 and R13 with no input signal applied. Note that the FRONT PANEL ZERO control R14 is split by the wiper arm action and added in series to R12 and R13. In operation, R14 zeros the buffer amplifier by adding in series either more or less than 375 ohms, i. e., one half of its value, to R12 or R13 to unbalance the amplifier enough to negate the initial offset voltage of Q1 and IC2A. Thus, when properly zeroed, the output of IC2A pin 7 is at the same potential as the input to Q1 on R11.

For DCV, ACV and OHMS measurements R18 is floating, i. e., contacts 3 and 6 of S2A are open. Q1 and IC2A now operate as a unity gain follower, independent of the setting of R17, so that the output of IC2A pin 7 is the same as the signal on contact 9 of S2A. For DCA and ACA measurements S2A contacts 3 and 6 close and R17 can now be adjusted to provide a resistance ratio of 9:1 in conjunction with R18 and R16 so that the buffer amplifier has a gain of 10. Thus independent of the RANGE or FUNCTION selected, the output of IC2A pin 7 always supplies 1 Volt for a full-scale input.

Capacitor C20 stabilizes the buffer amplifier by preventing excessive phase shifts due to parasitic capacitances in the feedback loop. D1 and D2 form a unidirectional zener of about 3.6V which restricts the output of IC2A from going below 3.6V for overrange input levels. Since the output of IC2A is short circuit proof and limited to 20mA source current, no damage results due to the hard zener clamp.

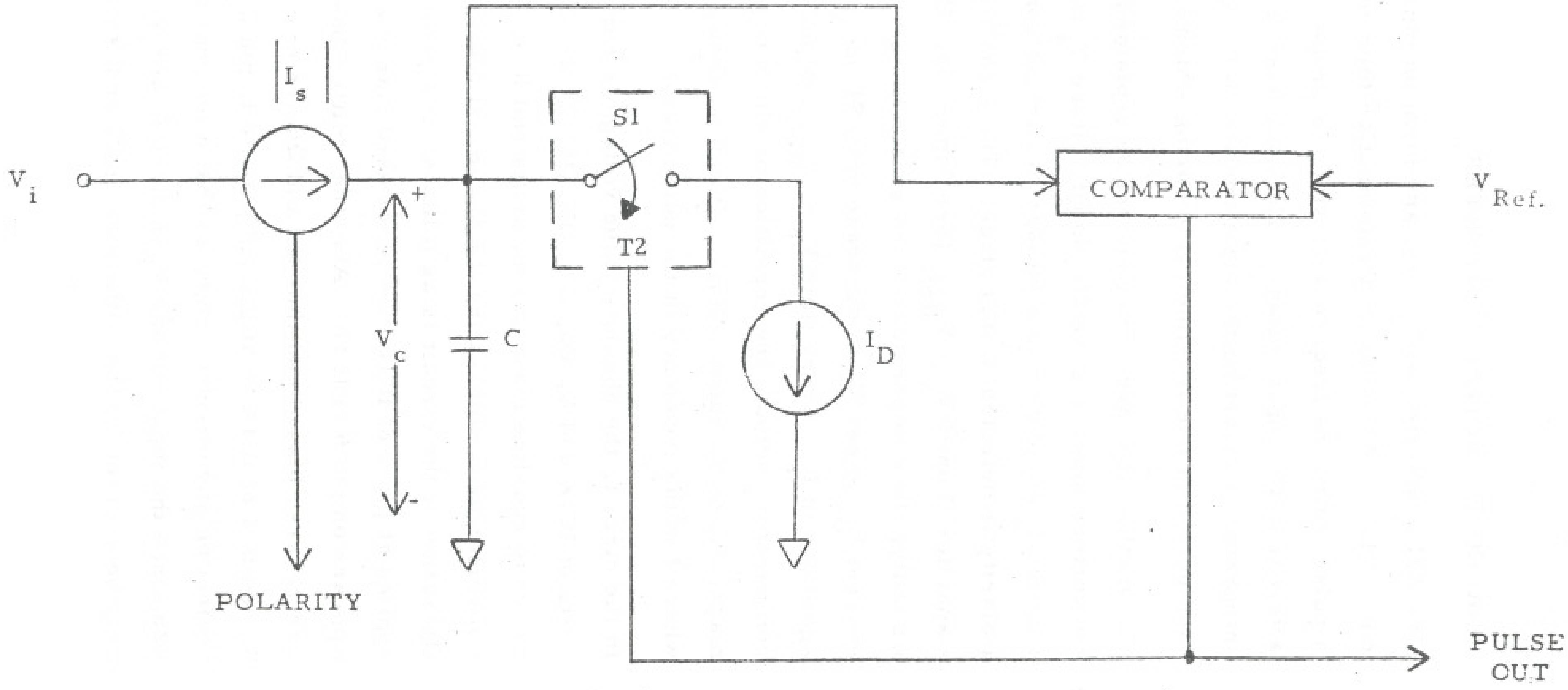
Overvoltage protection for Q1 is provided by the diode-connected FET Q2 which clamps to -9.4 Volts if the overvoltage is negative and by the Gate-Drain junction of Q1 itself if the signal at S2A contact 9 is above +9.6Volts. Thus when ±1500 Volts are applied to the input terminals with the 1V RANGE selected, R11 limits the current thru either FET junction to about 3.2mA.

C. ANALOG TO DIGITAL CONVERTER

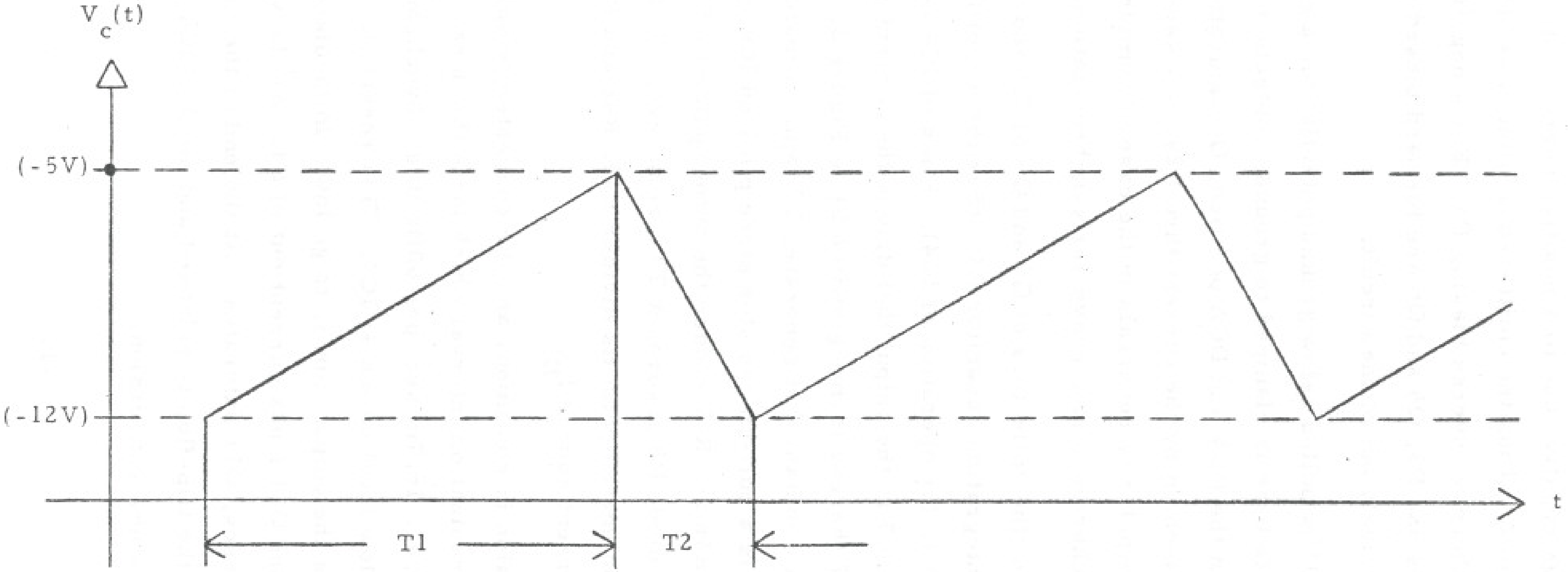
The A/D converter will accept any form on input voltage, i.e., "+" or "-" DC or AC volts or a combination thereof and convert it into a pulse train, the frequency of which is proportional to the absolute average of the input voltage. The converter is a true absolute value integrator, converting the input continuously except for a synchronization period of one AC-line cycle during which the converter is reset.

The method of conversion can best be explained by referring to the converter model (Figure 2). Input voltage V_i is converted into current I_s absolutely in a voltage to current converter. Also the polarity is detected in this stage. The signal current I_s charges capacitor C until $V_c = V_{Ref.}$ (See Figure 3). Upon detection of equality, the comparator closes switch S1 for a time T2. Discharge current I_D causes V_c to decrease until S1 opens and V_c increases again due to I_s. Every time $V_c = V_{Ref.}$, a pulse is produced at the comparators output, the repetition of which is proportional to the magnitude of the input voltage. It can be shown that $f = I_s/(I_D \times T_2)$ where f is the frequency of the pulse train.

In the circuit, the absolute value voltage to current converter consists of IC1A and B, D3, D4, Q5, Q6, Q7 and Q8. R15 and R22 serve to equalize bias current drifts and R21, R20 and R19 zero the converter by compensating for the initial offset voltage of IC1A and B. Operation of the circuit is as follows: If a positive input voltage is applied at pin 5 of IC1B, D4 is forward biased and the input voltage appears on pin 6 of IC1B. Also the emitter-base junctions of Q5 and Q6 are reverse biased and thus Q5 and Q6 are effectively out of the circuit. Since pin 3 of IC1A is at ground potential, pin 2 is also on ground, neglecting any offset voltage, so that a current I_s flows thru R25 and R26 since the input voltage V_i is directly across it. This current can only be sourced by the collectors of Q7 and Q8 since the output of



CONVERTER MODEL, FIGURE 2



T2 ≈ 37.4μ sec., T1 depends on input voltage

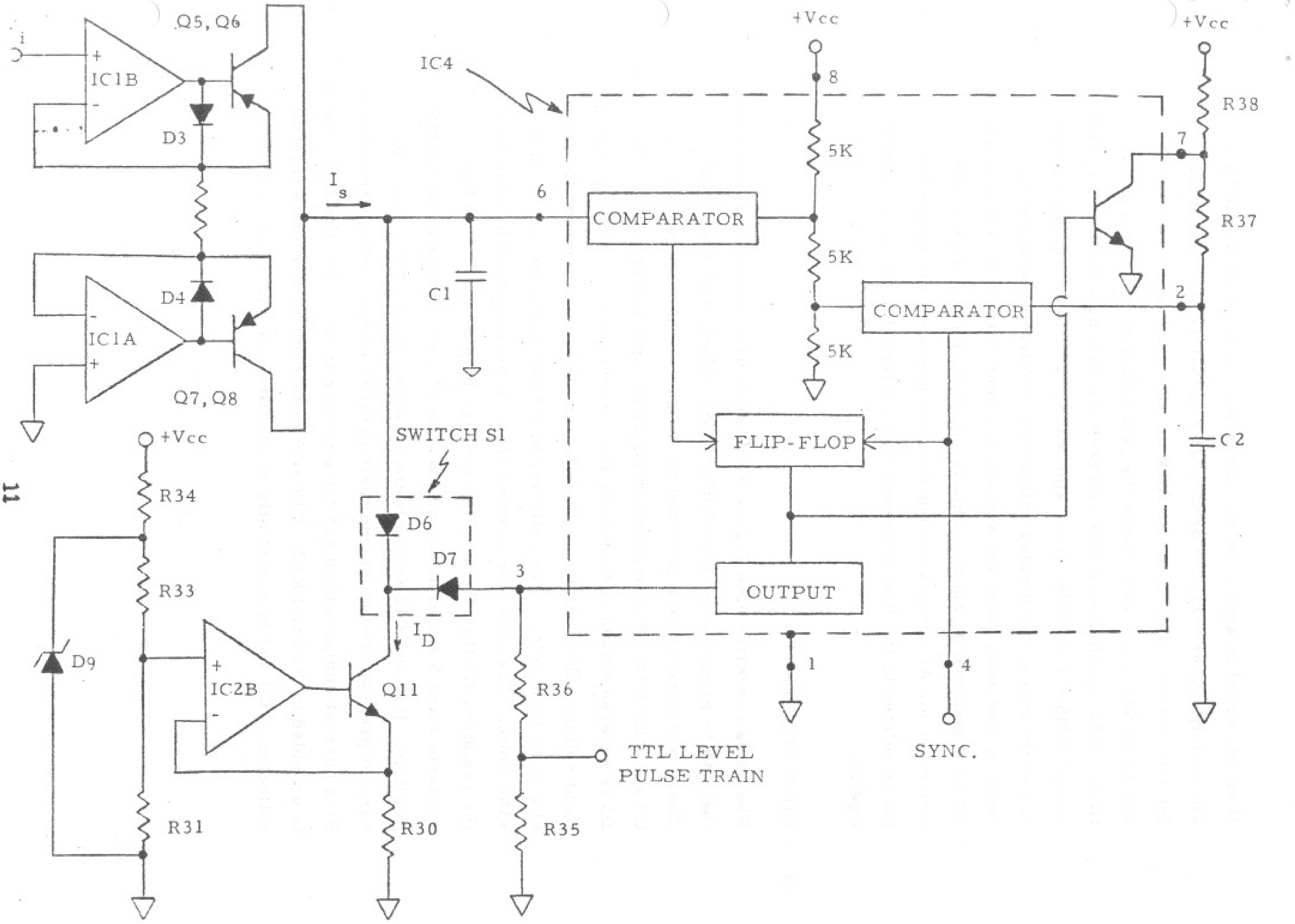
WAVEFORM ACROSS C1 (PIN 6 OF IC4), FIGURE 3

IC1A pin 1 swings negative due to a positive current into its inverting input terminal pin 2. Thus the emitter-base junctions of Q7 and Q8 are forward biased thereby reverse biasing D3. For a negative input the process reverses and D3, Q5 and Q6 are forward biased while D4, Q7 and Q8 are effectively out of the circuit.

The emitter of Q4 is pulled below ground potential for a negative input and since its base is clamped to ground, contacts 3 and 4 of S2A are closed in the DCV and DCA position, Q4 saturates and the minus sign is driven on by the current thru R29. C4 serves to filter out instantaneous polarity reversals in the case of complex signals and prevents flickering during converter synchronization.

The current out of the collectors of Q5 and Q6 or Q7 and Q8 now charges up the integrating capacitor C1. (See the simplified circuit diagram, Figure 4, for operation of IC4). Pin 6 of IC4 is the comparator input, pin 3 is the output that drives the current steering diodes D6 and D7 thereby forming switch S1 in Figure 2. R37 and C2 form the time constant that generates T2 (approximately 37.4μ seconds), R38 is a pull-up resistor since pin 7 on IC4 is driven low during T2. R36 and R35 reduce the output pulse to TTL levels and Germanium diode D8 assures a TTL zero level. IC2B, Q11, R30 and D9 in conjunction with its divider R33, R48 and R31 form the reference current source I_D.

Thus the conversion is continuous and the converter is only stopped during the synchronization interval which lasts the duration of one AC-line cycle, i.e., 16.7m sec. per 60Hz line. Synchronization is initiated by a low level on pin 4, IC4. This resets the flip-flop in IC4 and causes the output, pin 3, to go low. Immediately D6 is forward biased and Q11 sinks current out of C1. As the voltage across C1 decreases, Q11 saturates. At the end of the synchronization interval, the flip-flop is released and pin 3 of IC4 goes high thereby starting a new conversion.

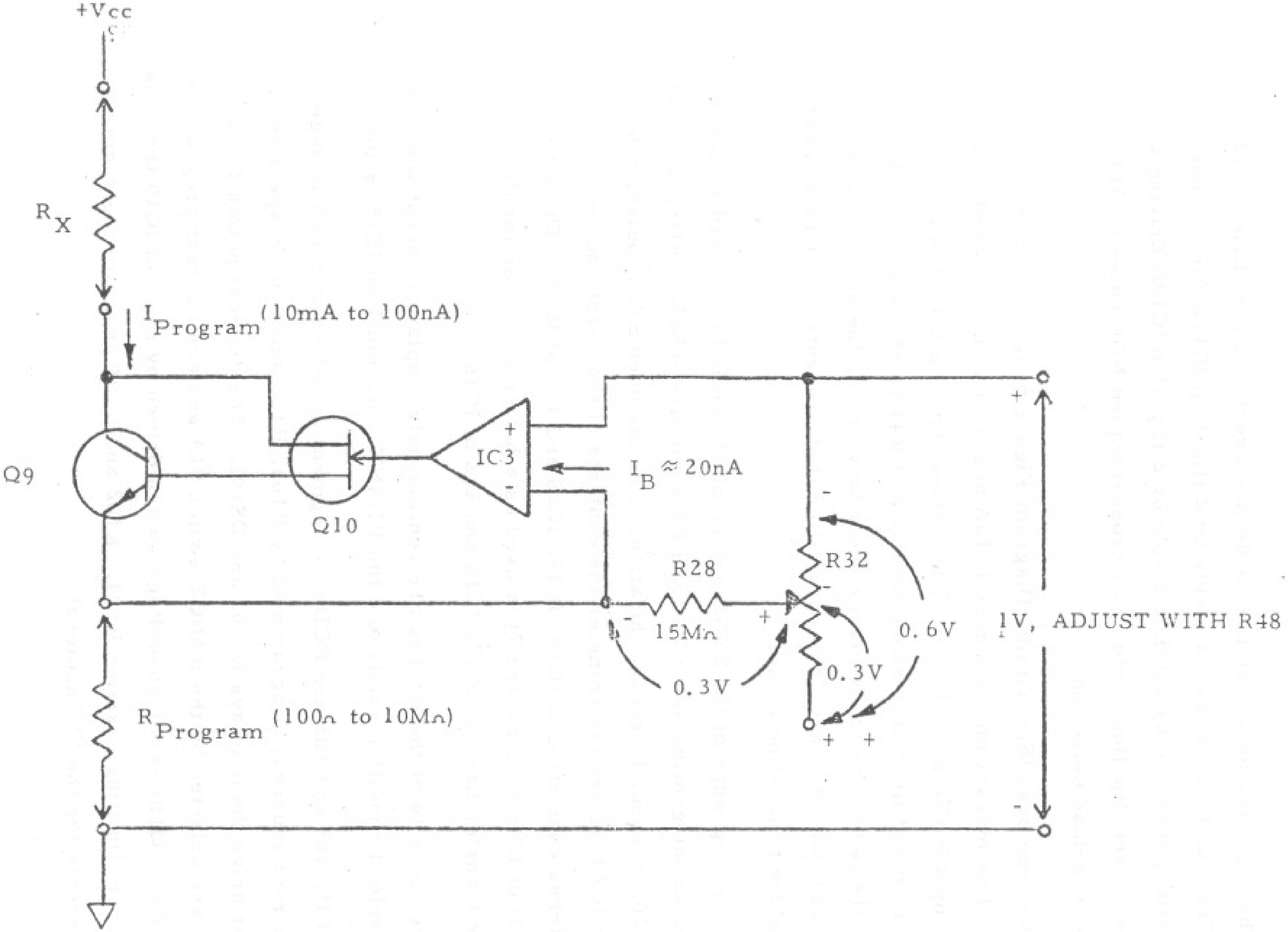


SIMPLIFIED CONVERTER CIRCUIT DIAGRAM, FIGURE 4

If an AC signal is applied at the converter input, IC1A and IC1B alternately flip and Q5, Q6 or Q7, Q8 alternately source current for integration. If S2 is in the ACV or ACA position, contacts 10 and 11 on S2A close and change the gain factor of the above amplifiers. R23 together with R24 increase the gain by a factor of 1.1105 since VRMS = 1.1105Vav for a sine wave. For low frequencies and full scale inputs, the display will not be steady, but will slowly count up and down about the average nominal reading by a maximum of approximately 4 counts. This is inherent in the design of the converter for AC integration but does not appear if the applied input is related to the line frequency by an integral number of quarter cycles.

D. OHMS CONVERTER

The ohms converter (See Figure 5) consists of a constant current sink that can be programmed for 10mA, 1mA, 100μA, 1μA and 100nA. These test currents are provided by the darlington configuration of Q9 and FET Q10. For accidential negative input voltages up to 250 Volts, D5 is reverse biased and protects the current source. For a positive input voltage, Q15 together with R47 protect Q10 by clamping the drain of Q10 to +0.6 Volts. The collector of Q9 can safely be pulled up to +300 Volts. The collector current of Q9 is programmed by switching the resistors R1 thru R6 into the feedback loop of IC3. Note that contacts 7 and 5 and also 12 and 1 & 2 of S2A are closed in the OHMS position. R49 and C18 decouple the inverting input of IC3 from the current program resistors and their parallel compensating capacitances. Bias current compensation and temperature tracking for the 10MΩ range is provided by R28 and R32. C19 serves to remove any noise from the collector of Q9 and is essentially in parallel with the unknown resistor.



SIMPLIFIED OHMS CONVERTER CIRCUIT DIAGRAM, FIGURE 5

E. DIGITAL LOGIC AND DISPLAY

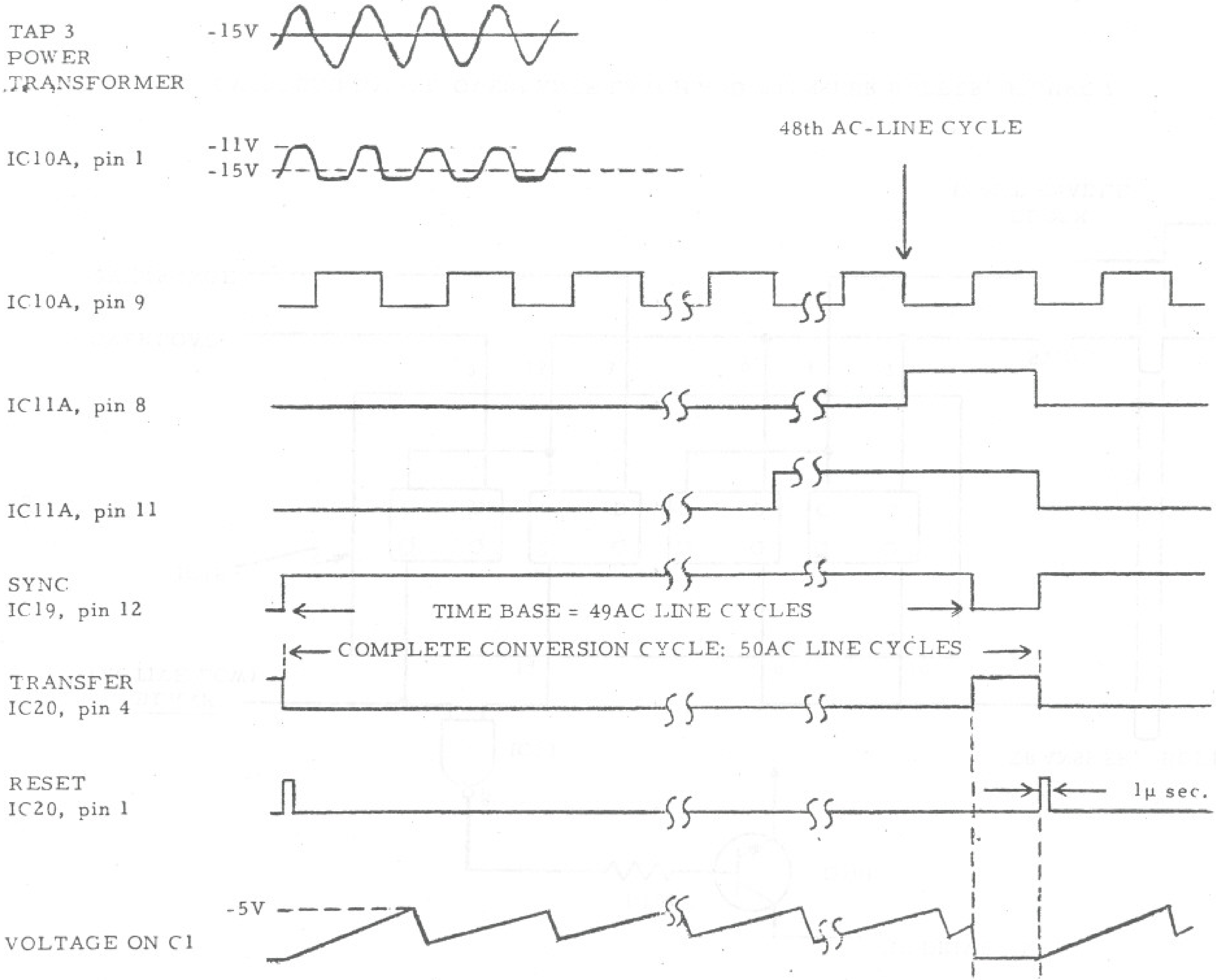
The logic section consists of a decade event counter chain, IC12, IC13, IC14 followed by a divide by 2 flip-flop IC11B for "1" indication, followed by another divide by 2 flip-flop IC10B driving a set-reset flip-flop made up of cross-coupled NOR gates (IC20) for overload detection.

The time base (See Timing Diagram Figure 6) is derived from the AC line by cascaded dividers IC10A and IC11A and decoded by the 3 input NAND gate (IC19). The divider input, pin 1 on IC10A, is driven and limited in swing by D20 and R43 to +3.9V and -0.6V, by the tap on the transformer secondary, i.e., the anode of D16. In addition, R43 and C5 form a filter that prevents spurious triggering due to AC-line noise.

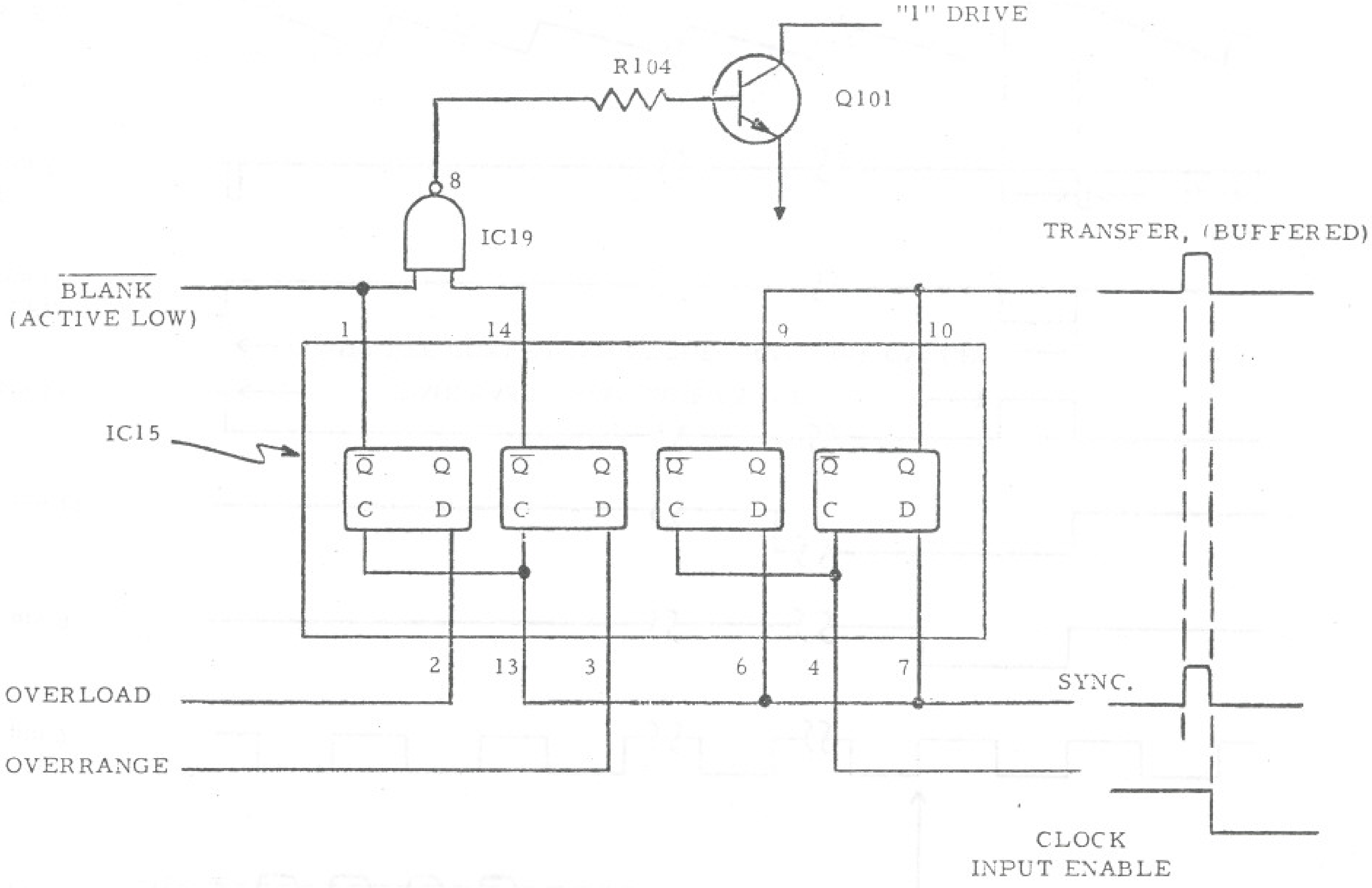
The rising edge of the SYNC pulse, pin 12 on IC19, is used to generate via an integrating delay R44 and C3 a positive RESET pulse, pin 1 on IC20, of about 1μ second duration. The inverted SYNC pulse, pin 4 on IC20, is used to transfer the contents of the event counter into latches consisting of IC16, IC17, IC18 and 1/2 of IC15. The other half of IC15 (See Figure 7) is used as a buffer amplifier for driving the transfer lines of IC17, IC18 and 1/2 of IC16.

The contents of the latches are continuously displayed except when an overload condition exists and the BLANK line, pin 1 on IC15 is low.

IC101, 102 and 103 are BCD to 7 segment decoders and high voltage current sources, programmed by R105, R106 and R107 respectively, that drive the displays DS101 and DS102. The decimal points P1 thru P4 are selected by the RANGE switch S1A and are current programmed by R40. Q101 is a high-voltage switch driven by pin 8 of IC19 thru base current limiting resistor R104. R102 and R103 program the segment currents for the "1" numeral.



282 TIMING DIAGRAM, FIGURE 6



OVERLOAD LATCH, OVERRANGE LATCH AND TRANSFER BUFFER, FIGURE 7

F. POWER SUPPLY

The power supply generates 5 regulated voltages. Series pass regulation is provided for the +180V display supply and for the 5 Volt logic supply; zener shunt regulation supplies +9V, -15V and -18V.

Q13 together with R41 and D15 forms a low impedance emitter follower output. C15 eliminates zener noise that could couple into the input buffer amplifier via the decimal point switch. R45 is a current limiting resistor, protecting the outputs of IC101, IC102 and IC103.

The analog supply levels +9V, -15V and -18V are dropped across zener diodes D12, D13 and D14 which are driven by the current limiting resistor R42. C13 across D13 suppresses transients during the SYNC time interval when Q11 in the reference current source saturates and IC2B, via the +9V supply, has to source 8.7mA. Bypassing is provided on all three supplies by C7, C8 and C9.

The 5V logic supply has its "ground" at the -15 Volt analog level so that the +5 Volt appears as -10 Volts with respect to common ground, i.e., the cathode of D13. The darlington Q14 gets its base drive from the 6.2V reference zener D9 so that the voltage across bypass capacitor C6 is 5 Volts.

2. TEST AND CALIBRATION PROCEDURE

The following procedure should be used whenever recalibration becomes necessary due to service or repair of the unit. The sequence of tests must be exactly as outlined below to insure that the unit meets all specifications.

A. WARM UP

Remove top and bottom cover, then plug unit into AC-outlet. Switch FUNCTION to DCV and set RANGE to 1V. Do not apply any inputs. Let unit warm up for about 10 minutes before proceeding with Step B.

B. CONVERTER ZERO

FUNCTION: DCV
RANGE : 1V
INPUT : None

Jumper cathode of D1 to cathode of D2. Adjust R19 for ".000" on display with <u>flickering minus sign</u>. (This is the exact center of zero.) Remove jumper.

C. FRONT PANEL ZERO

FUNCTION: DCV
RANGE : 1V
INPUT : Short "+" to "com"

Adjust wiper of R14 (zero control on front panel) to center of pot. If positive reading is displayed on meter, add appropriate resistor (See Table 1) in parallel with R12. If reading is negative add resistor in parallel with R13.

TABLE 1

36 counts add 51K
30 counts add 62K
24 counts add 75KΩ
18 counts add 110KΩ
12 counts add 150KΩ
9 counts add 220KΩ
6 counts add 300KΩ

After addition of resistor meter should read between ±3 counts.

D. RAMP LEVEL CHECK

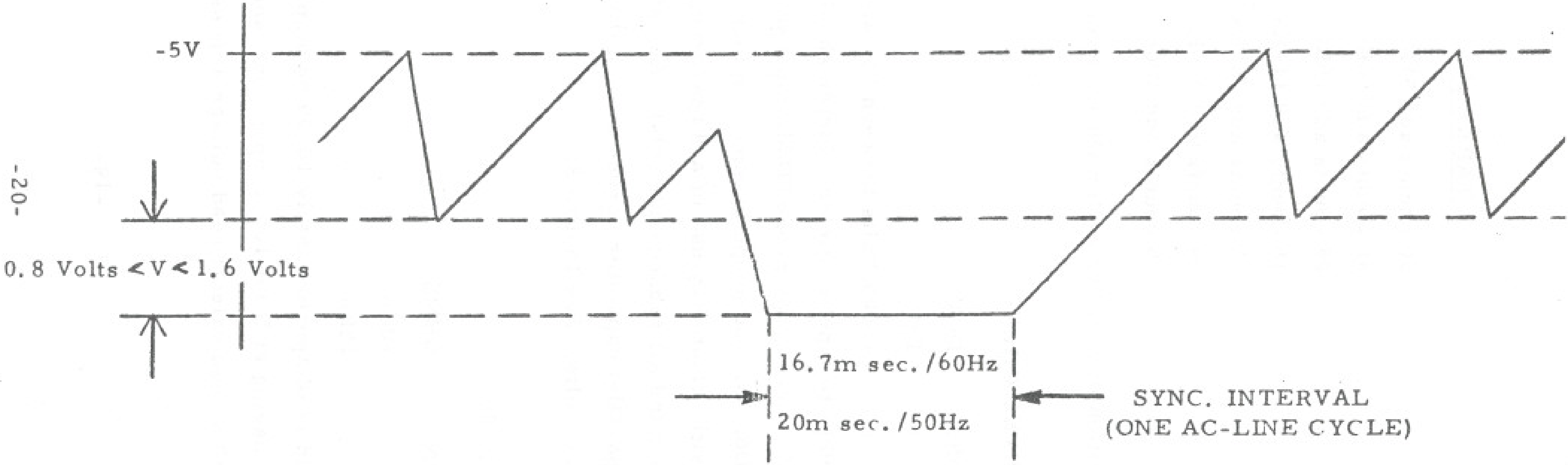
FUNCTION: DCV
RANGE : 10V
INPUT : 1.000 Volts between "+" and "com"

Apply 1.000V to input of meter. Meter should read approximately "1.00". Connect scope probe (10MΩ input impedance minimum) to anode of D6. Ground scope to input common terminal. (NOTE: Scope must be floated by use of a three-prong adapter on line cord in this and all subsequent tests). Adjust C1 if necessary by adding a parallel capacitor across it such that "V" is between 0.8 and 1.6 Volts. See Figure 8.

E. OHMS ADJUST

FUNCTION: OHMS
RANGE : 10KΩ
INPUT : 10KΩ

Unit should read approximately 10.00 on display. With external voltmeter having at least 10MΩ input impedance (Data Precision Model 2450 or equivalent) read voltage across input terminals.



RAMP LEVEL CHECK WAVE FORM, FIGURE 8

Adjust R48 such that external meter reads "1.000" Volts ±0.5mV. NOTE: A parallel resistor may be necessary across R31 or R33 to obtain this "1.000" reading.

Remove external voltmeter. Change meter function to DCA and zero meter with front panel zero pot. This is a true meter zero.

Change meter function switch back to OHMS. Adjust R25 for reading of "10.00" on unit under test.

Set RANGE to 10MΩ and connect a 10MΩ ±.1% resistor across "+" and "com" terminals. Adjust R32 for a reading of "10.00".

Return to 10KΩ position and with 10KΩ across input readjust R25 if necessary.

Check all other OHMS ranges with appropriate .1% resistors across inputs.

All readings should be 1000 ±10 counts, with the exception of 100Ω range (due to test lead resistance).

Ohms Protection

FUNCTION: OHMS

RANGE : 100Ω

Apply ±250VDC or 180VRMS to input terminals for 3 seconds. Recheck 100Ω range.

F. DC VOLTS

FUNCTION: DCV

RANGE : 1V

Short "+" and "com" terminals. Meter should read ".000". If not, go back to Step 1. Apply 1.000VDC, and adjust R48 for a reading of "1.000".

Lower line voltage with variac to 105VAC. Reading should not vary more than ±1 count. .Return to117VAC.

Switch RANGE to 10V. Apply 10.00VDC to inputs, meter should read "10.00" ±5 counts after a minimum of 3 seconds. Apply 100VDC to 100VDC RANGE and 1000VDC to 1000VDC RANGE. Readings should be "100.0" ±5 counts and "1000." ±10 counts respectively.

Apply 1000VAC to DC 1 Volt RANGE. Go back and check 1VDC range.

G. DC CURRENT

FUNCTION: DCA

RANGE lmA

Short "+" and "com" terminals and adjust front panel zero for ".000" reading. Remove short and apply 1.000mADC to input terminals. Adjust R17 for "1.000" reading. Check 10mA, 100mA and 1A RANGES with appropriate input. Readjust R17 if necessary such that no range reads more than 1000 ±10 counts.

Overload Protection

FUNCTION: DCA

RANGE : lmA

Apply ±100mA to input terminals. If voltage drop across input terminals is greater than 1 Volt, D10 (- voltage) or D11 (+ voltage) is not functioning.

H. AC VOLTS

FUNCTION: ACV

RANGE : 1VAC

a) Apply 1.000RMS @ 1KHZ to input terminals. Adjust R24 for "1.000" reading.

b) RANGE: 10V. Apply 10.00VRMS @ 1KHZ. Adjust C21 for "10.00" reading. A 10pf capacitor across C21 may be necessary in order to get a reading of "10.00".

c) RANGE: 100V. Apply 100.0VRMS @ 1KHZ to input terminals. Select C22 such that a reading of "100.2" is obtainable by adjusting C23.

d) RANGE: 1000V. Apply 500VRMS @ 1KHZ to input terminals. Select C25 for a reading of "505." ±1 count.

e) Repeat Steps b) through d) as necessary.

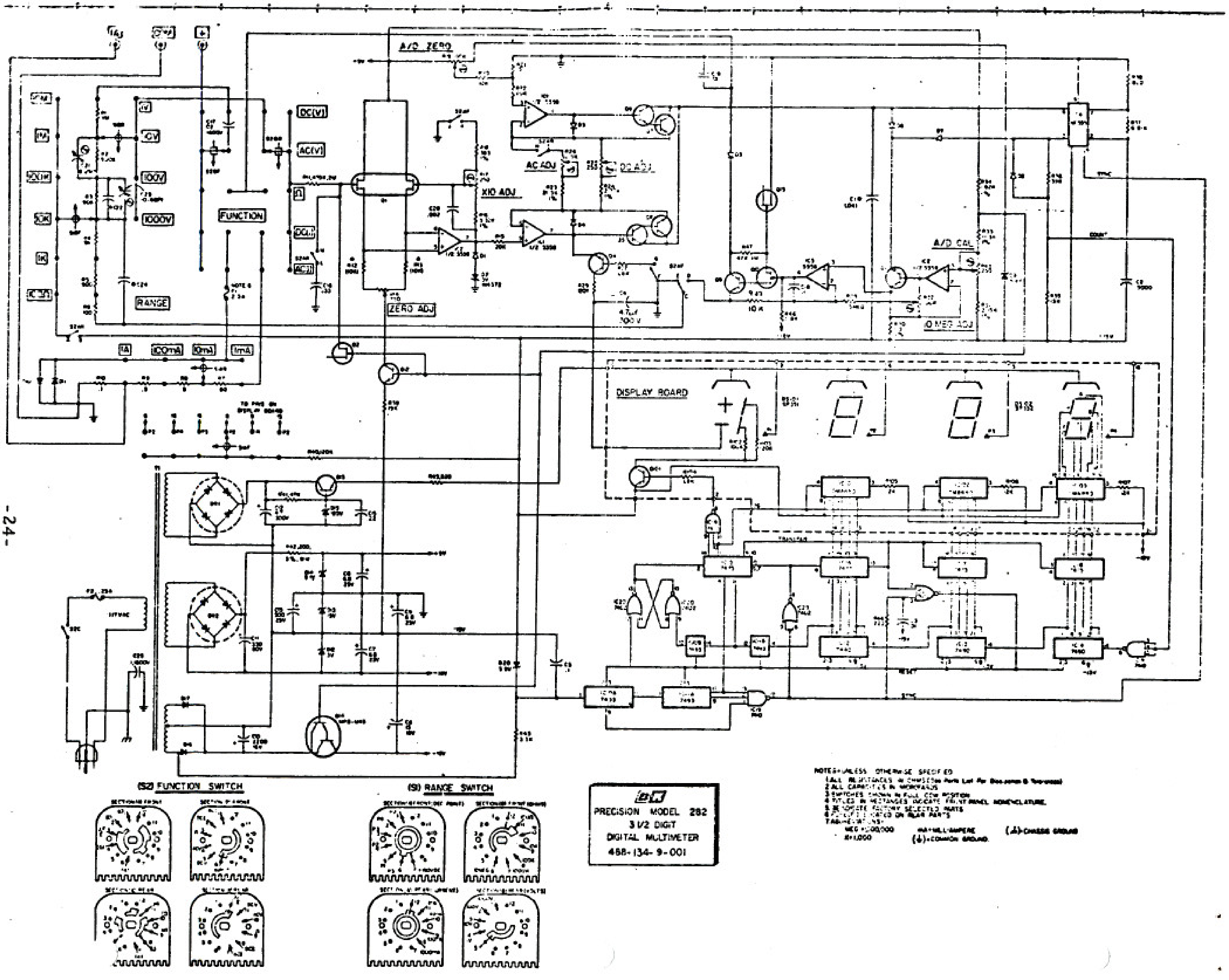
f) Apply 1000VRMS @ 1KHZ to 1VAC range for 3 seconds. Meter must overrange. Apply 1.000VRMS @ 1KHZ to 1VAC range. Meter should read "1.000".

I. AC CURRENT

FUNCTION: ACI

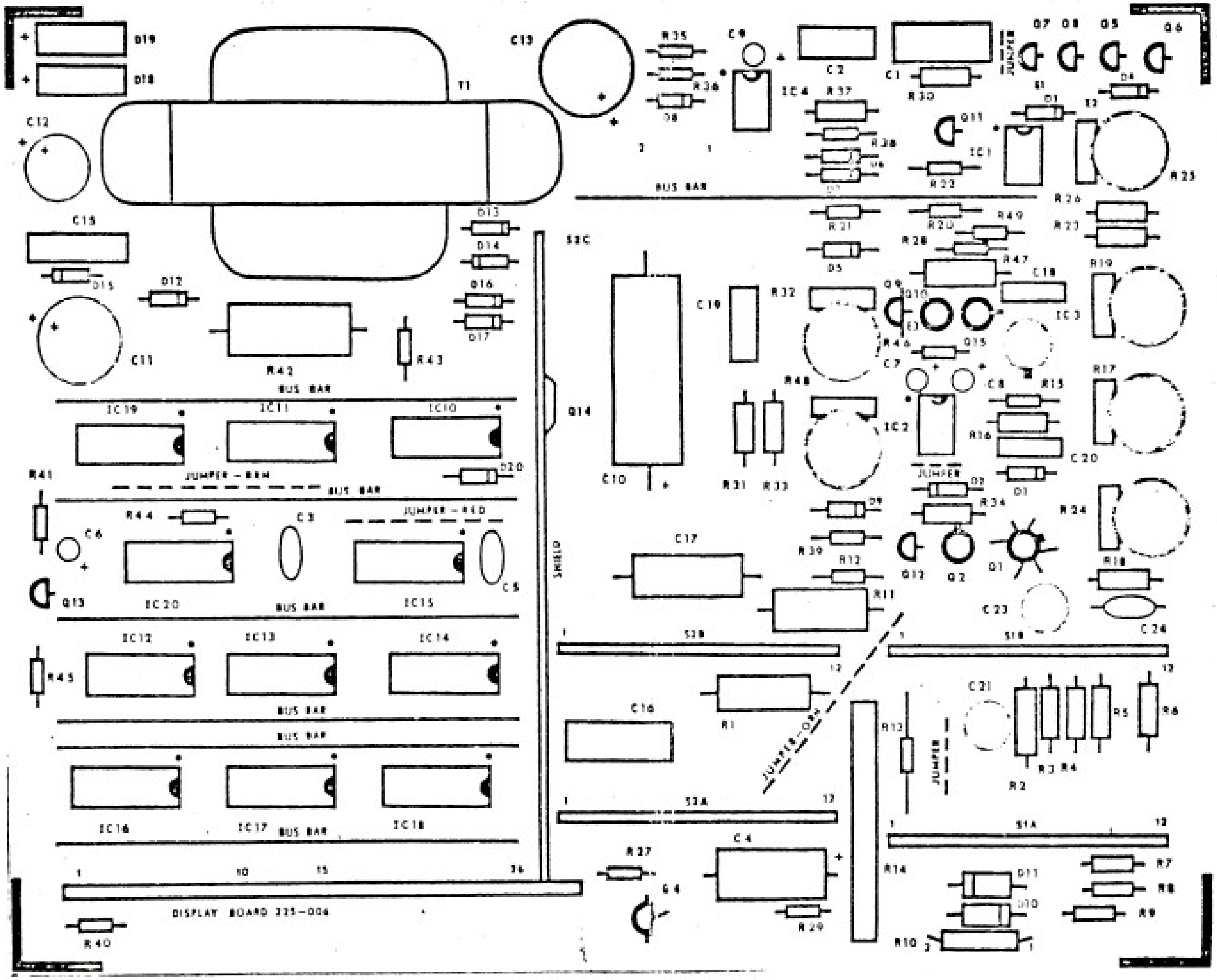
RANGE : 1mA

Apply 1.000mARMS @ 1KHZ to inputs. Meter should read "1.000" ±10 counts. This reading will depend on the 1mA DC current setting via R17.



B&K PRECISION MODEL 282
3 1/2 DIGIT
DIGITAL MULTIMETER
488-134-9-001

NOTES:-UNLESS OTHERWISE SPECIFIED
1 ALL RESISTANCES IN OHMS (See Parts List for Tolerance & Wattage)
2 ALL CAPACITORS IN MICROFARADS
3 SWITCHES SHOWN IN FULL CCW POSITION
4 TITLES IN RECTANGLES INDICATE FRONT PANEL NOMENCLATURE.
5 [illegible] DENOTE FACTORY SELECTED PARTS
6 [illegible] LOCATED ON REAR PANEL
7 ABBREVIATIONS-
MEG =1,000,000 mA=MILLIAMPERE (⏊)=CHASSIS GROUND
K=1,000 (⏚)=COMMON GROUND.



COMPONENT LAYOUT