Headers for connection to front panel PCB.

ECO#	REV:	DESCRIPTION	REV. BY:	DATE
6935	A00	RELEASE TO PRODUCTION	KR	4-16-04
7042	A01	CHANGE FPGA TO PREPROGRAMMED PART	SDPL	5-13-04
7159	B00	CHANGE RESISTOR VALUES AND S1B LANDS FOR AMOI	SDPL	7-1-04

END OF BOARD NEAREST POWER SWITCH

DGND [1,11,12,13,14,15,16,17,18] → J14-1
DGND [1,11,12,13,14,15,16,17,18] → J14-2
+5V [1,11,12,13,14,15,16,17,18] → J14-3
+5V [1,11,12,13,14,15,16,17,18] → J14-4
FPGA_LED_32KHZ [16] → J14-5
FPGA_LED_44.1KHZ [16] → J14-6
FPGA_LED_48KHZ [16] → J14-7
FPGA_LED_88.2KHZ [16] → J14-8
FPGA_LED_96KHZ [16] → J14-9
FPGA_LED_176.4KHZ [16] → J14-10
FPGA_LED_192KHZ [16] → J17-1
FPGA_LED_EXTERNAL [16] → J17-2
FPGA_LED_LOCK [16] → J17-3
+3.3V [1,11,12,15,16,17] → J17-4
+3.3V [1,11,12,15,16,17] → J17-5
ENCODER_BIT0 [16] → J17-6
ENCODER_BIT1 [16] → J17-7
ENCODER_BIT2 [16] → J17-8
SW_24_16 [16] → J17-9
+15V_M [1,15] → J17-10
+15V_M [1,15] → J17-11
+15V_M [1,15] → J17-12
+15V_M [1,15] → J17-13
MGND [1,15] → J17-14
MGND [1,15] → J17-15
MGND [1,15] → J17-16
-15V_M [1,15] → J17-17
-15V_M [1,15] → J17-18
-15V_M [1,15] → J17-19
PGND [1,15] → J17-20
CHGND_2 [1,8,9,15] — C592 .1uF — AGND_CH1 [2,10,11,15] → J18-1
GAIN_SND_CH1 [2] → J18-2
GAIN_RET_CH1 [2] → J18-3
PHNT_CNTRL_CH1 [2] → J18-4
PHASE_0_CH1 [2] → J18-5
PHASE_180_CH1 [2] → J18-6
PHASE_SWOUT_CH1 [2] → J18-7
HPF_OUTPUT_CH1 [2] → J18-8
HPF_SWOUT_CH1 [10] → J18-9
N.C. → J18-10
CHGND_2 [1,8,9,15] — C787 .1uF — AGND_CH2 [3,10,11,15] → J18-11
GAIN_SND_CH2 [3] → J18-12
GAIN_RET_CH2 [3] → J18-13
PHNT_CNTRL_CH2 [3] → J18-14
PHASE_0_CH2 [3] → J18-15
PHASE_180_CH2 [3] → J18-16
PHASE_SWOUT_CH2 [3] → J18-17
HPF_OUTPUT_CH2 [3] → J18-18
HPF_SWOUT_CH2 [10] → J18-19
N.C. → J18-20
CHGND_2 [1,8,9,15] — C792 .1uF — AGND_CH3 [4,12,15] → J20-1
GAIN_SND_CH3 [4] → J20-2
GAIN_RET_CH3 [4] → J20-3
PHNT_CNTRL_CH3 [4] → J20-4
PHASE_0_CH3 [4] → J20-5
PHASE_180_CH3 [4] → J20-6
PHASE_SWOUT_CH3 [4] → J20-7
HPF_OUTPUT_CH3 [4] → J20-8
SPLITOUT_CH3 [4,12] → J20-9
CHGND_2 [1,8,9,15] — C793 .1uF — N.C. → J20-10
AGND_CH4 [5,12,15] → J21-1
GAIN_SND_CH4 [5] → J21-2
GAIN_RET_CH4 [5] → J21-3
PHNT_CNTRL_CH4 [5] → J21-4
PHASE_0_CH4 [5] → J21-5
PHASE_180_CH4 [5] → J21-6
PHASE_SWOUT_CH4 [5] → J21-7
HPF_OUTPUT_CH4 [5] → J21-8
SPLITOUT_CH4 [5,12] → J21-9
CHGND_2 [1,8,9,15] — C794 .1uF — N.C. → J21-10
AGND_CH5 [6,13,15] → J22-1
GAIN_SND_CH5 [6] → J22-2
GAIN_RET_CH5 [6] → J22-3
PHNT_CNTRL_CH5 [6] → J22-4
PHASE_0_CH5 [6] → J22-5
PHASE_180_CH5 [6] → J22-6
PHASE_SWOUT_CH5 [6] → J22-7
HPF_OUTPUT_CH5 [6] → J22-8
SPLITOUT_CH5 [6,13] → J22-9
CHGND_2 [1,8,9,15] — C795 .1uF — N.C. → J22-10
AGND_CH6 [7,13,15] → J23-1
GAIN_SND_CH6 [7] → J23-2
GAIN_RET_CH6 [7] → J23-3
PHNT_CNTRL_CH6 [7] → J23-4
PHASE_0_CH6 [7] → J23-5
PHASE_180_CH6 [7] → J23-6
PHASE_SWOUT_CH6 [7] → J23-7
HPF_OUTPUT_CH6 [7] → J23-8
SPLITOUT_CH6 [7,13] → J23-9
CHGND_2 [1,8,9,15] — C796 .1uF — N.C. → J23-10
AGND_CH7 [8,14,15] → J23-11
GAIN_SND_CH7 [8] → J23-12
GAIN_RET_CH7 [8] → J23-13
PHNT_CNTRL_CH7 [8] → J23-14
PHASE_0_CH7 [8] → J23-15
PHASE_180_CH7 [8] → J23-16
PHASE_SWOUT_CH7 [8] → J23-17
HPF_OUTPUT_CH7 [8] → J23-18
SPLITOUT_CH7 [8,14] → J23-19
CHGND_2 [1,8,9,15] — C797 .1uF — N.C. → J23-20
AGND_CH8 [9,14,15] → J24-1
GAIN_SND_CH8 [9] → J24-2
GAIN_RET_CH8 [9] → J24-3
PHNT_CNTRL_CH8 [9] → J24-4
PHASE_0_CH8 [9] → J24-5
PHASE_180_CH8 [9] → J24-6
PHASE_SWOUT_CH8 [9] → J24-7
HPF_OUTPUT_CH8 [9] → J24-8
SPLITOUT_CH8 [9,14] → J24-9
N.C. → J24-10

END OF BOARD NEAR HI-Z INPUTS.

B1 ☐ 0012143-04 RND BUTTON CAP (7MM) "LINE" WHITE BOTTOM
B2 ☐ 0012143-04 RND BUTTON CAP (7MM) "LINE" WHITE BOTTOM
B3 ☐ 0012143-04 RND BUTTON CAP (7MM) "LINE" WHITE BOTTOM
B6 ☐ 0012143-04 RND BUTTON CAP (7MM) "LINE" WHITE BOTTOM
B7 ☐ 0012143-04 RND BUTTON CAP (7MM) "LINE" WHITE BOTTOM
B8 ☐ 0012143-04 RND BUTTON CAP (7MM) "LINE" WHITE BOTTOM
B9 ☐ 0012143-04 RND BUTTON CAP (7MM) "LINE" WHITE BOTTOM
B11 ☐ 0012143-04 RND BUTTON CAP (7MM) "LINE" WHITE BOTTOM

B10 ☐ 0012143-06 RND BUTTON CAP (7MM) "GUITAR" (symbol) WHITE BOTTOM
B12 ☐ 0012143-06 RND BUTTON CAP (7MM) "GUITAR" (symbol) WHITE BOTTOM

B13 ☐ 0012143-07 RND BUTTON CAP (7MM) CONTROL GRAY TOP WHITE BOTTOM
B14 ☐ 0012143-07 RND BUTTON CAP (7MM) CONTROL GRAY TOP WHITE BOTTOM
B15 ☐ 0012143-07 RND BUTTON CAP (7MM) CONTROL GRAY TOP WHITE BOTTOM
B16 ☐ 0012143-07 RND BUTTON CAP (7MM) CONTROL GRAY TOP WHITE BOTTOM
B17 ☐ 0012143-07 RND BUTTON CAP (7MM) CONTROL GRAY TOP WHITE BOTTOM

Z100 ☐ 0007714-01 PCB FAB Onyx 800R Main

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APPROVALS	DATE
DRAWN: SDPL	12/09/03
CHECKED:	
NP ENG:	
MATERIAL:	
MFG:	
MFG ENG:	
ISSUED:	

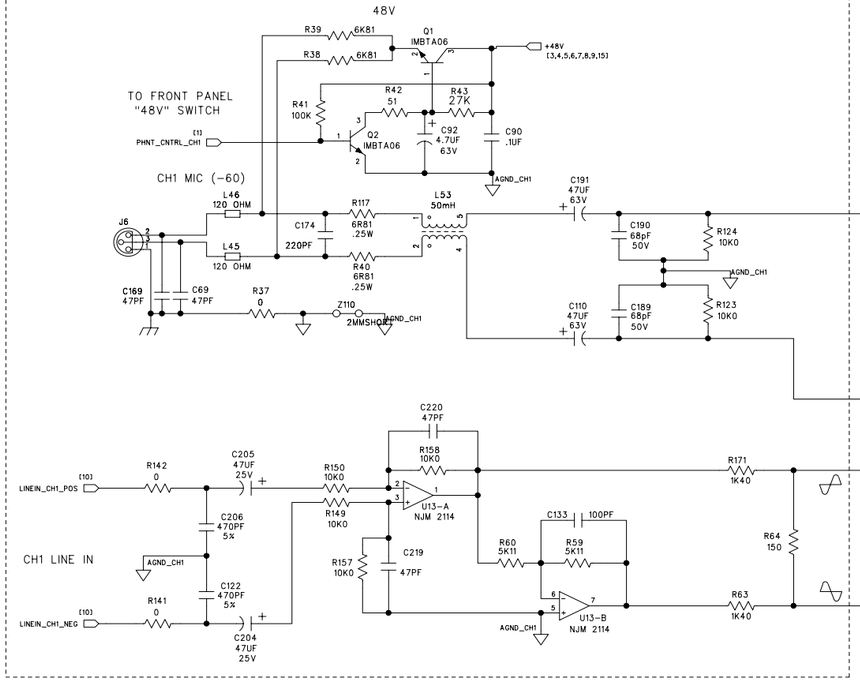
Mackie Designs Inc. Woodinville, Wa.

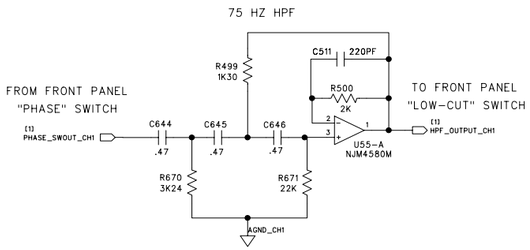
ONYX 800R: MAIN

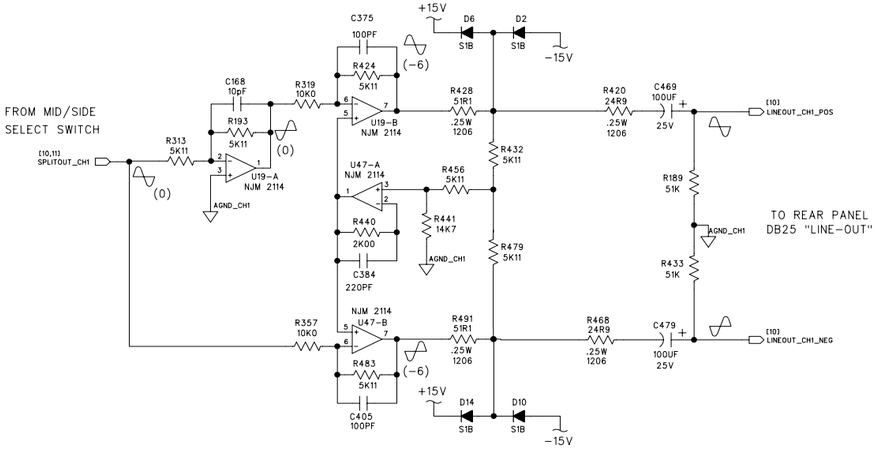
SIZE D | SCALE: NONE | DWG. NO. SCH0007715-00 | REV. B00
DWG FILE: | SHEET 1 OF 18

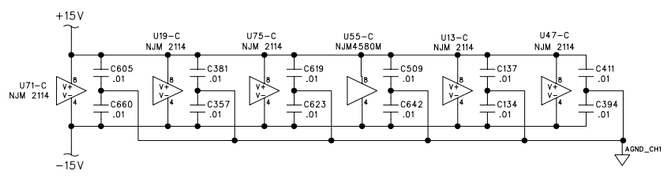
CHANNEL 1

LOCATE NEAR BACK PANEL – CLOSE TO ENTRY POINT









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Mackie Designs Inc. Woodinville, Wa.

ONYX 800R: MAIN

SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715–00	B00
DWG FILE:		SHEET 2 OF 18	

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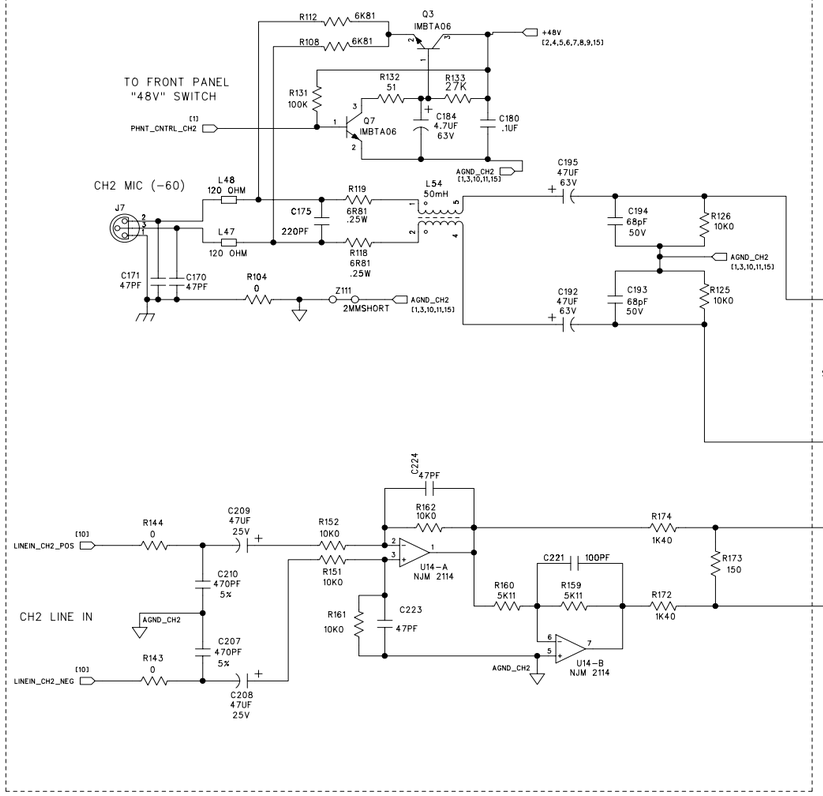
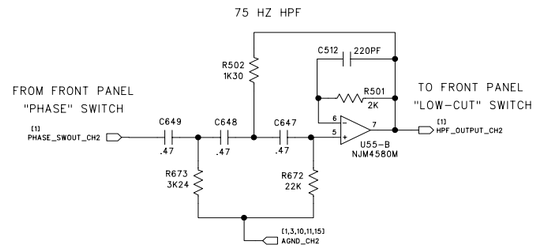
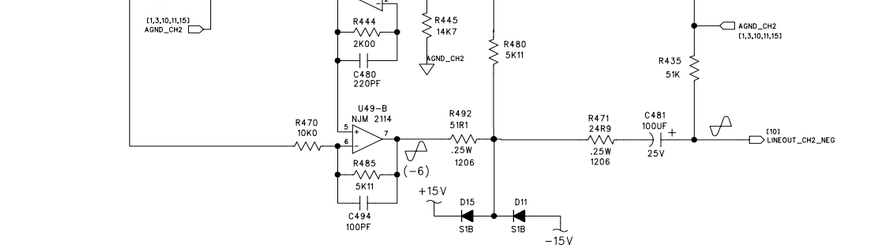
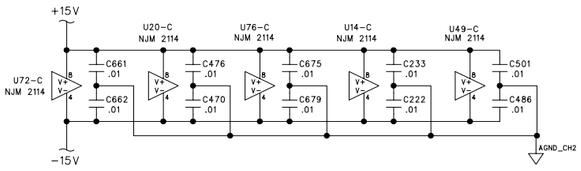
CHANNEL 2

LOCATE NEAR BACK PANEL – CLOSE TO ENTRY POINT









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ONYX 800R: MAIN

SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715-00	B00
DWG FILE:		SHEET 3 OF 18	

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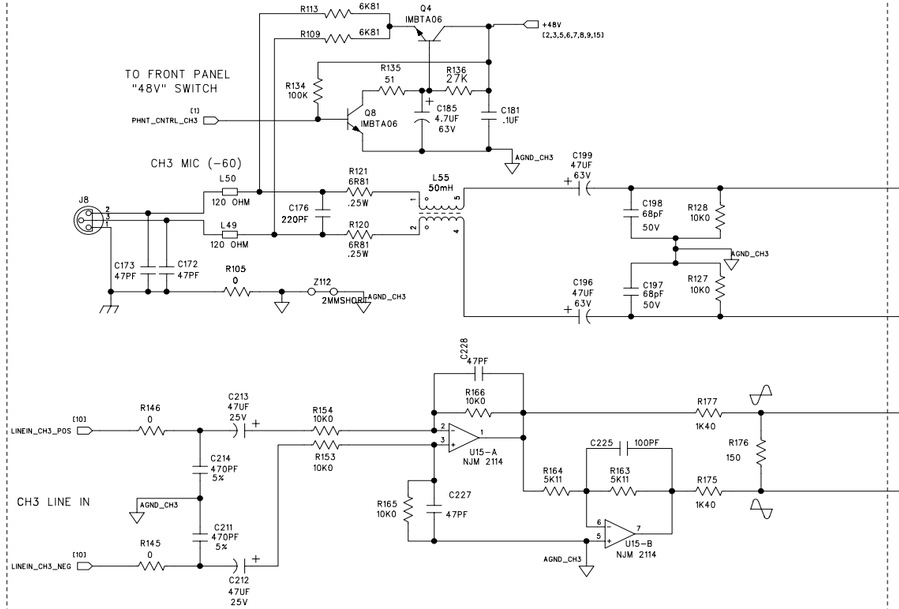
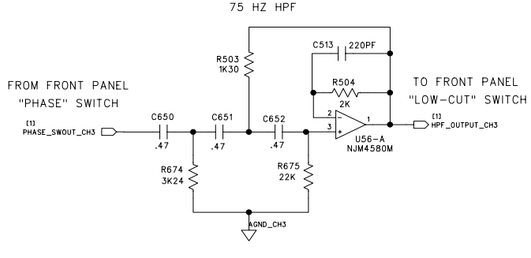
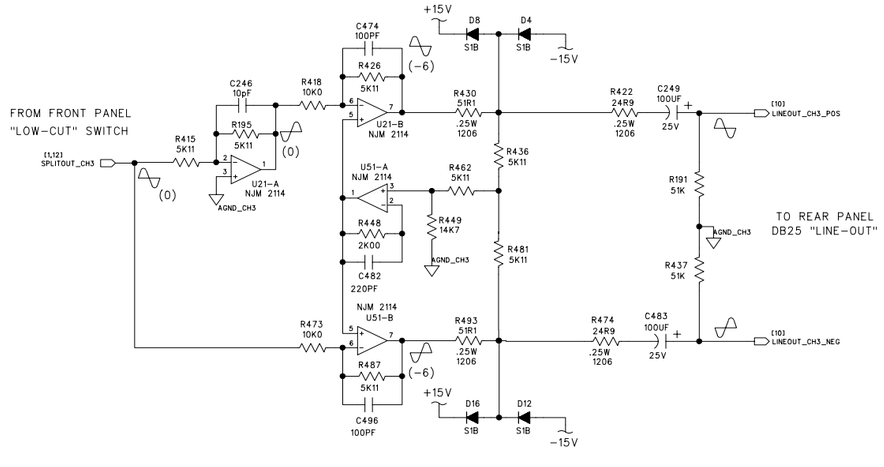
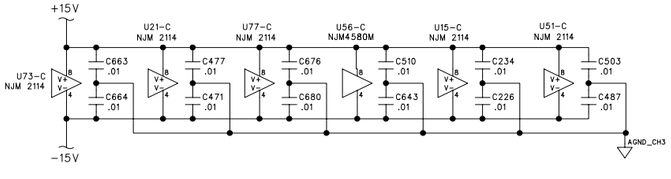
CHANNEL 3

LOCATE NEAR BACK PANEL – CLOSE TO ENTRY POINT









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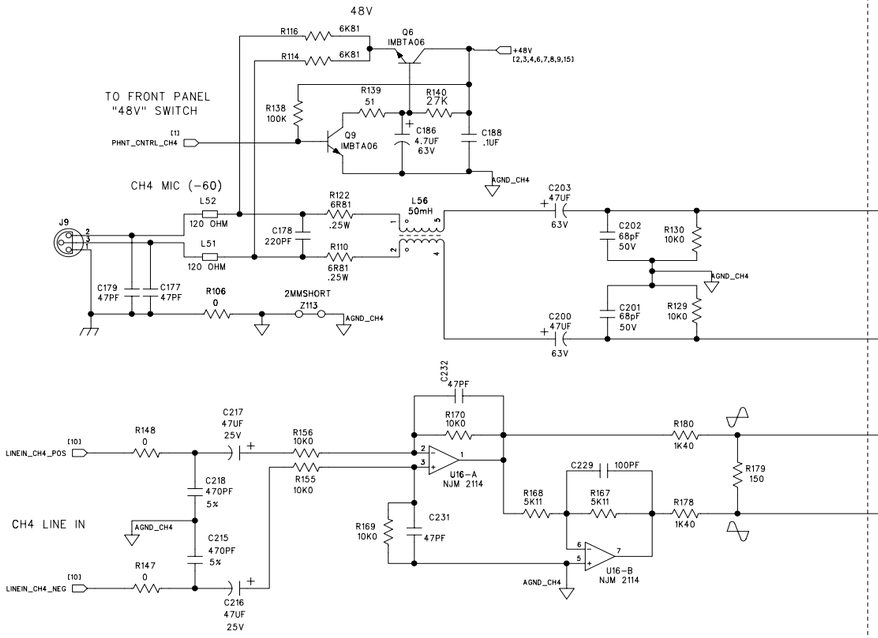
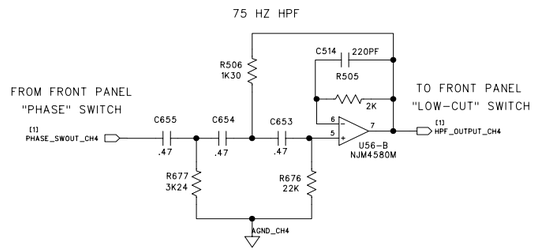
ONYX 800R: MAIN

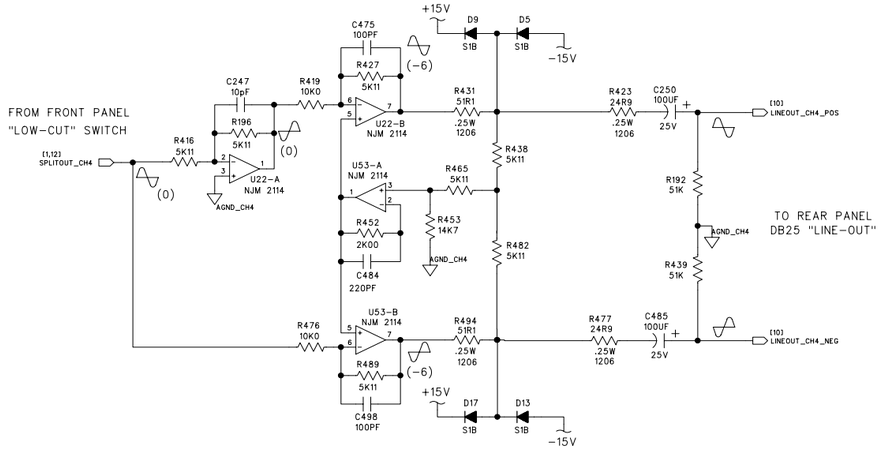
SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715-00	B00
DWG FILE:		SHEET 4 OF 18	

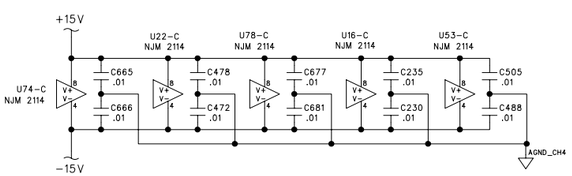
CHANNEL 4

LOCATE NEAR BACK PANEL – CLOSE TO ENTRY POINT









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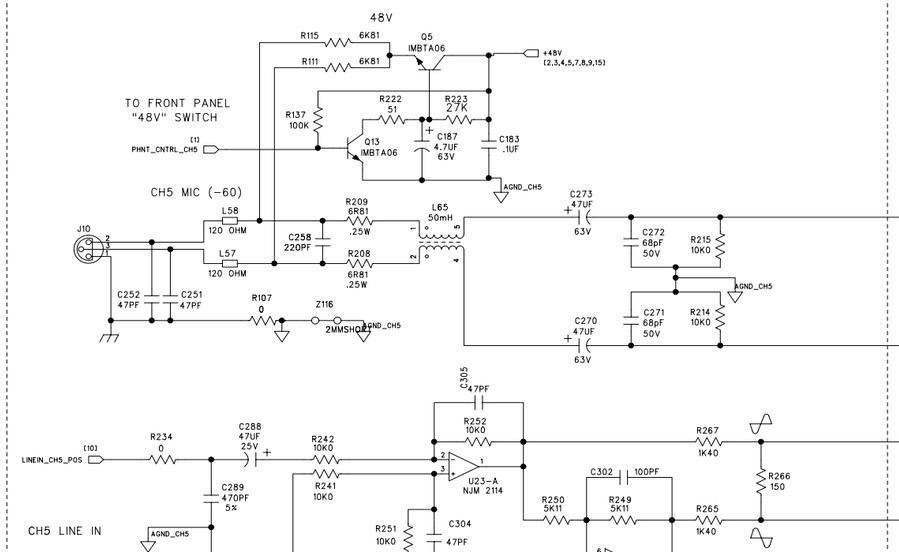
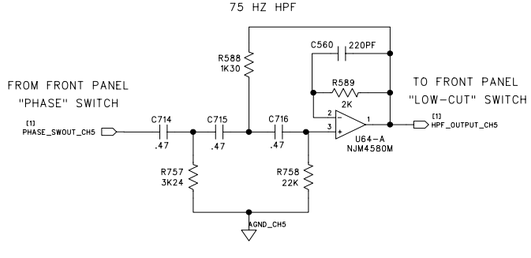
ONYX 800R: MAIN

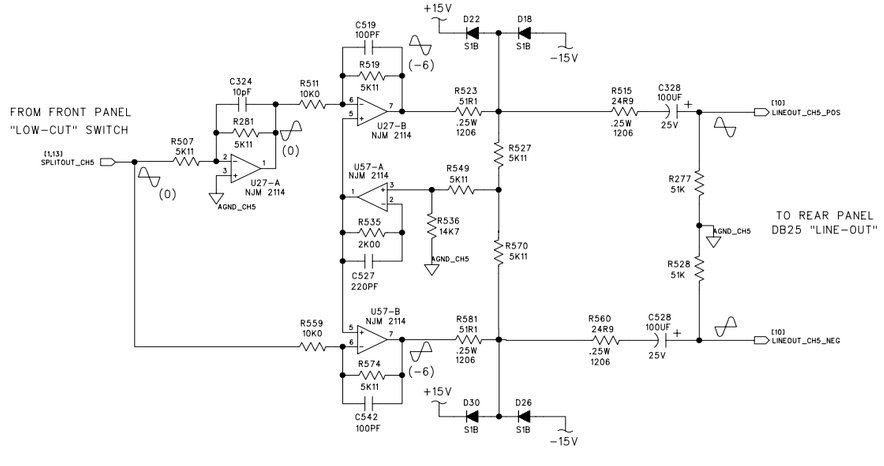
SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715-00	B00
DWG FILE:		SHEET 5 OF 18	

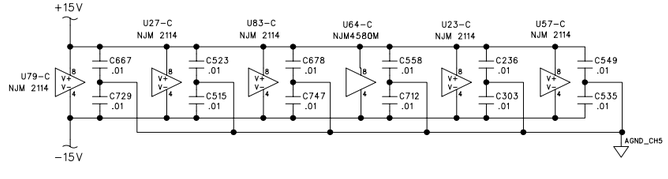
CHANNEL 5

LOCATE NEAR BACK PANEL – CLOSE TO ENTRY POINT









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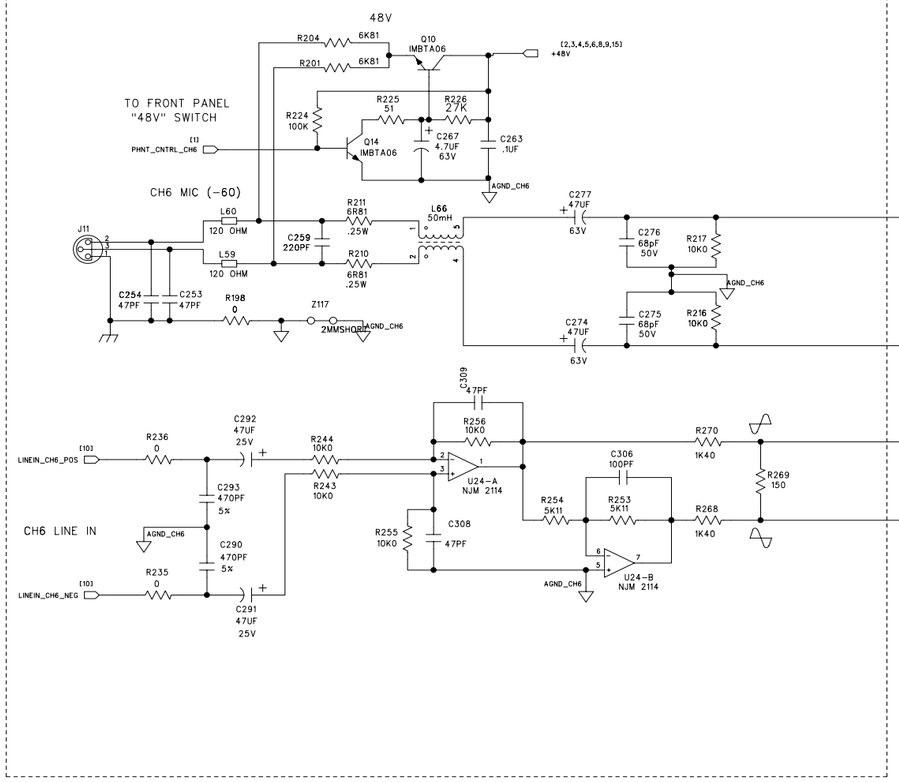
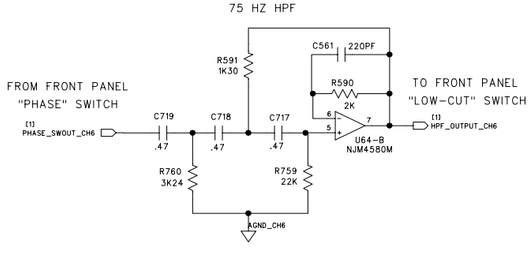
ONYX 800R: MAIN

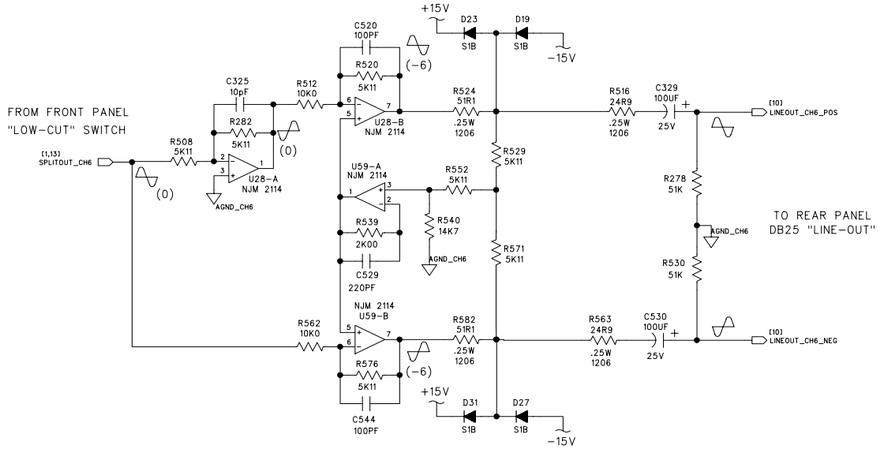
SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715-00	B00
DWG FILE:		SHEET 6 OF 18	

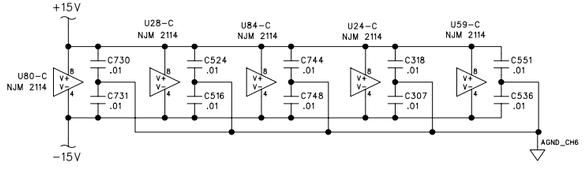
CHANNEL 6

LOCATE NEAR BACK PANEL – CLOSE TO ENTRY POINT









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ONYX 800R: MAIN

SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715-00	B00
DWG FILE:		SHEET 7 OF 18	

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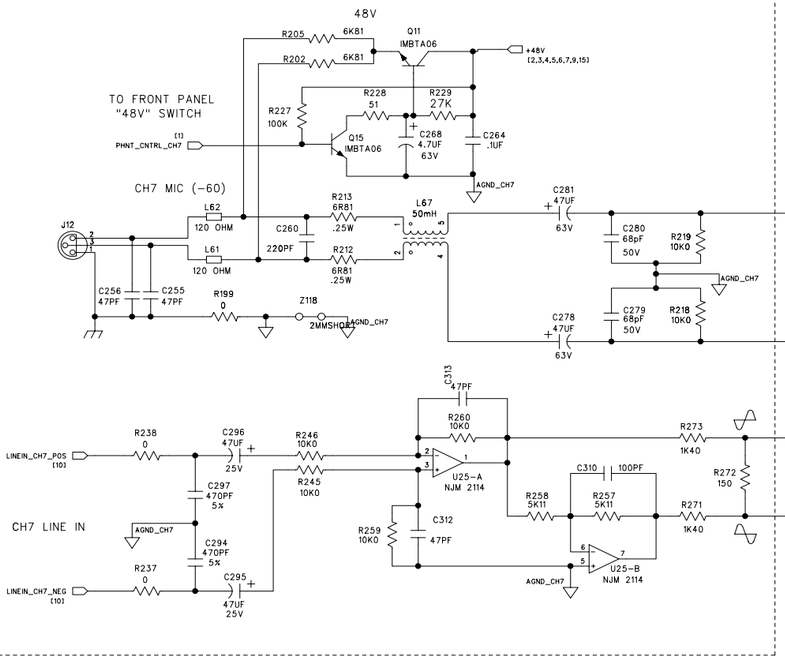
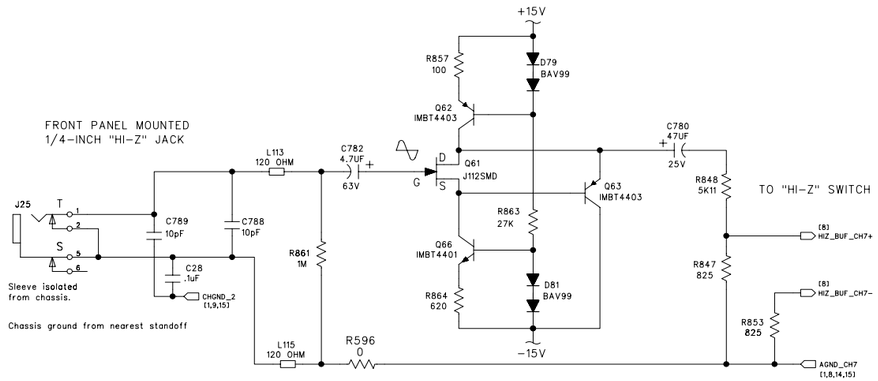
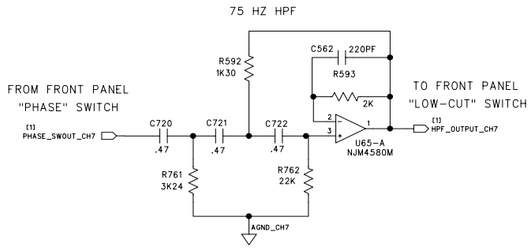
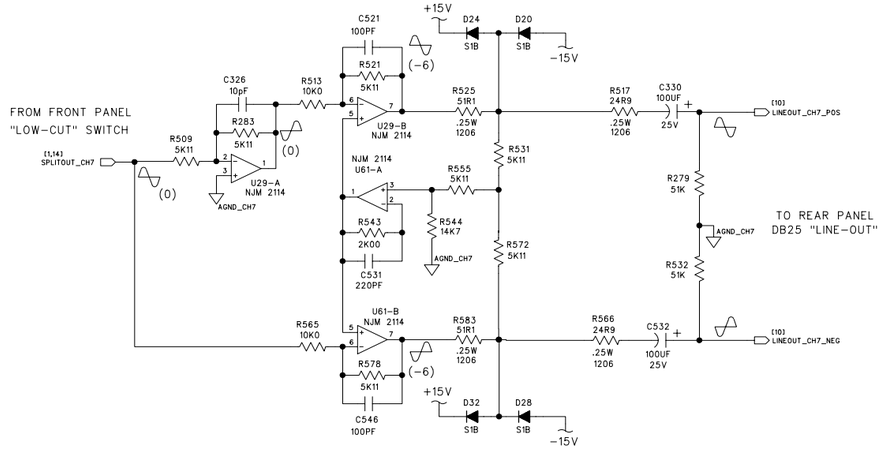
CHANNEL 7

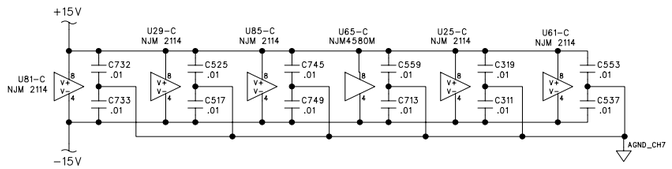
LOCATE NEAR BACK PANEL – CLOSE TO ENTRY POINT











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ONYX 800R: MAIN

SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715-00	B00
DWG FILE:		SHEET 8 OF 18	

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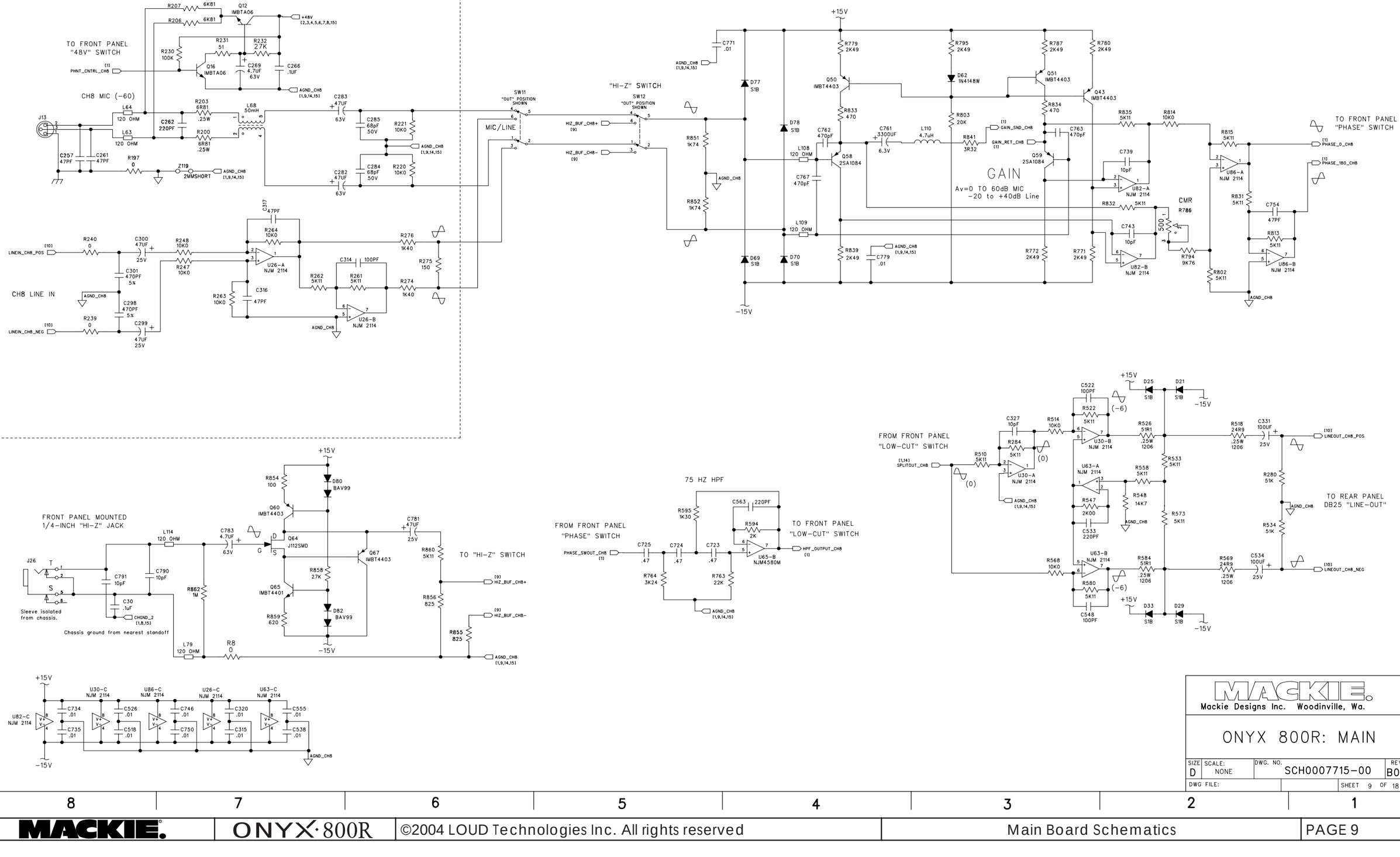
CHANNEL 8

LOCATE NEAR BACK PANEL – CLOSE TO ENTRY POINT

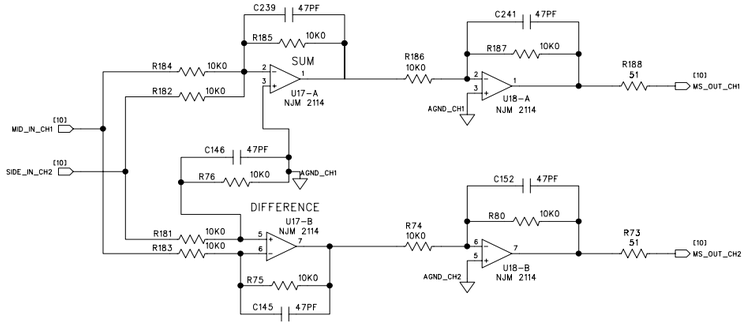


Mackie Designs Inc. Woodinville, Wa.

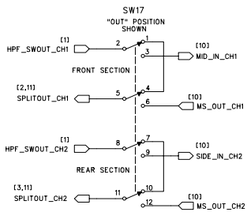
ONYX 800R: MAIN

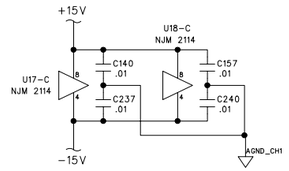
SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715–00	B00
DWG FILE:		SHEET 9 OF 18	

MID/SIDE MATRIX

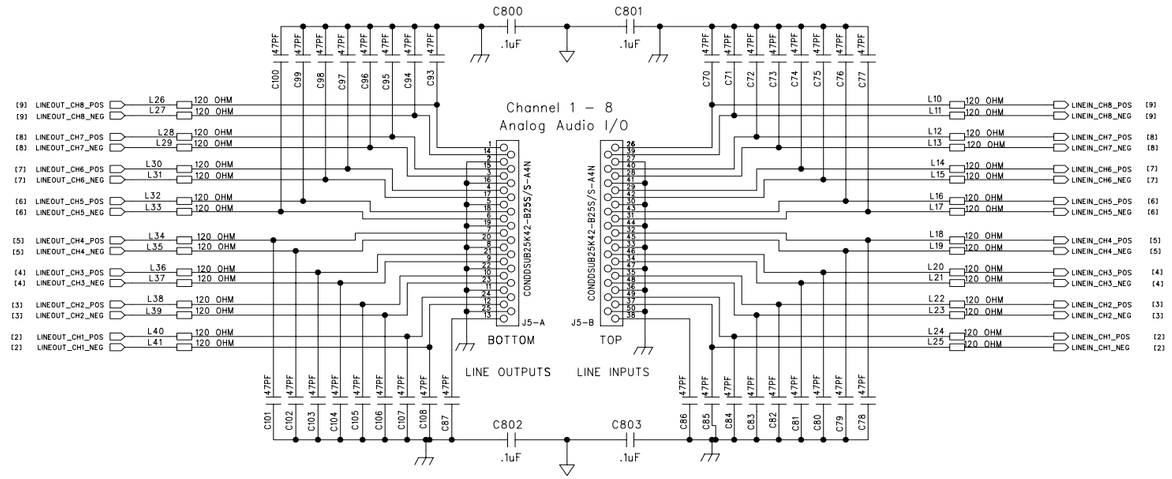


NORMAL MODE – SWITCH UP
MID–SIDE MODE – SWITCH DOWN





ANALOG I/O HEADERS



Mackie Designs Inc. Woodinville, Wa.

ONYX 800R: MAIN

SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715–00	B00
DWG FILE:		SHEET 10 OF 18	

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A-TO-D CHANNELS 1 & 2

PLACE OVER AGND PLANE

LOCATE ALONG CHANNELS

LOCATE ALONG AGND/DGND EDGE

+15V
U35-C NJM 2114
U48-C NJM 2114
C410 .1uF
C500 .1uF
C399 .1uF
C489 .1uF
AGND_CH1
AGND_CH2
-15V

C404 47PF
R364 5K11
U35-B NJM 2114
R370 5K11
AGND_CH1
C129 47UF 25V
R57 1K00
{11,12,13,14,15} +5VA
R44 4K75
BIAS
C115 10UF 50V
C118 .1uF
R46 4K75
C119 47UF 25V
R49 1K00
R56 10K0
R48 10K0
U7-A NJM 2114
U7-B NJM 2114
R55 178 1%
R45 178 1%
C121 1.8NF
R47 100
(-14)
R356 5K11
R343 5K11
R353 10K0
{2,10} SPLITOUT_CH1
U35-A NJM 2114
R352 5K11
R342 5K11
AGND_CH1

FROM REAR PANEL "MID/SIDE" SWITCH

C493 47PF
R484 5K11
U48-B NJM 2114
R495 5K11
AGND_CH2
C163 47UF 25V
R98 1K00
{11,12,13,14,15} +5VA
R68 4K75
BIAS
C144 10UF 50V
C150 .1uF
R79 4K75
C151 47UF 25V
R93 1K00
R97 10K0
R92 10K0
U10-A NJM 2114
U10-B NJM 2114
R96 178 1%
R72 178 1%
C156 1.8NF
R91 100
(-14)
R469 5K11
R443 5K11
R458 10K0
{3,10} SPLITOUT_CH2
U48-A NJM 2114
R457 5K11
R442 5K11
AGND_CH2

PLACE OVER DGND PLANE

C124 .22
AK5385VS-SO28
VCOM OVT W/S DFS1 DFS0 CKS1 CKS0 DIF HPFE PDN
VREFL LIN+ LIN- RIN+ RIN- VREFR
LRCK BICK MCLK SDTO
TEST AVDD AVSS_1 AVSS_2 AVSS_3 DVDD DVSS BVSS
C158 .22
C148 0.1uF
C154 10UF 16V
C127 0.1uF
C120 10UF 16V
C114 470UF 10-16V
C132 0.1uF
C142 0.1uF
C165 470UF 10-16V
C155 10UF 16V
C149 0.1uF
L44 120 OHM
{11,12,13,14,15} +5VA
REMOVE FERRITE BEAD IF PLACING AK5394. 470UF OPTION REDUCES LOW-FREQ THD+N
R62 0 Remove for AK5394
R66 0 Remove for AK5394
Remove .22uf for AK5385?
L42 120 OHM
+5V
R54 0 Remove for AK5394
C125 10UF 16V
C159 10UF 16V
R71 0 Remove for AK5394
BRING THICK DGND TRACE THRU SINGLE POINT, THEN JOIN WITH AGND CLOSE TO EACH CONVERTER.
Z105 1MMSHORT
Z106 2MMSHORT
{12,13,14} DGND_ADCS

+5V
R67 10K
OPEN (HIGH) WHEN PLACING AK5394A
R69 0
R70 1K0
CKS1_12
C808 .1uF
C117 47PF
{12,13,14} ADC_DFS1
{12,13,14} ADC_DFS0
{12,13,14} ADC_CKS0
{12,13,14} ADC_PDN
1Hz HI-PASS ENABLE HIGH
R78 10K
SERIAL AUDIO FORMAT - MSB JUSTIFIED
R52 10K
SLAVE MODE
R53 10K
C111 .1uF
C31 47PF
C141 .1uF
C113 47PF
{12,13,14} ADC_LRCK
{12,13,14} ADC_BCLK
ADC0_SDTO
{12,13,14} ADC_MCLK
C354 .1uF
C131 47PF
Capactively couple DGND and AGND where these four clock-like nets cross between. Keep routed together. Cross gap only once.

+5V
C123 0.1uF
VCC GND
U5 74HCT245
DIR OE
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
R51 1K0
LOW SETS B AS INPUTS
R50 1K0
ADC_CONFIG_DFS1 {16}
ADC_CONFIG_DFS0 {16}
ADC_CONFIG_CKS0 {16}
ADC_CONFIG_PDN {16}
DELAY PDN RISE FOR ADC SETTLING

ADC0_ERROR_FLAG
{12} ADC1_ERROR_FLAG
{13} ADC2_ERROR_FLAG
{14} ADC3_ERROR_FLAG
U42-B 74LVC32
U42-A 74LVC32
U42-C 74LVC32
COMBINE ERROR FLAGS TO ONE SIGNAL
R388 430
C432 0.1uF
D1 RED
U42-D 74LVC32

+5V
C126 .1uF
GND VCC
U6-G 74ACT14

+3.3V
C427 .1uF
VCC GND
U42-E 74LVC32

ADC_LRCK
ADC_BCLK
ADC_MCLK
R61 51
R58 51
R65 51
U6-B 74ACT14
U6-A 74ACT14
U6-D 74ACT14
U6-C 74ACT14
U6-F 74ACT14
U6-E 74ACT14
{16} FPGA_LRCK_OUT
{16} FPGA_BCLK_OUT
{16} FPGA_MCLK_OUT
U9-A 74LVC32
R95 51
{16} ADCO_SDTO_FPGA

+15V
U7-C NJM 2114
U10-C NJM 2114
C116 .1uF
C128 .1uF
C143 .1uF
C162 .1uF
-15V

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ONYX 800R: MAIN

SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715-00	B00
DWG FILE:		SHEET 11 OF 18	

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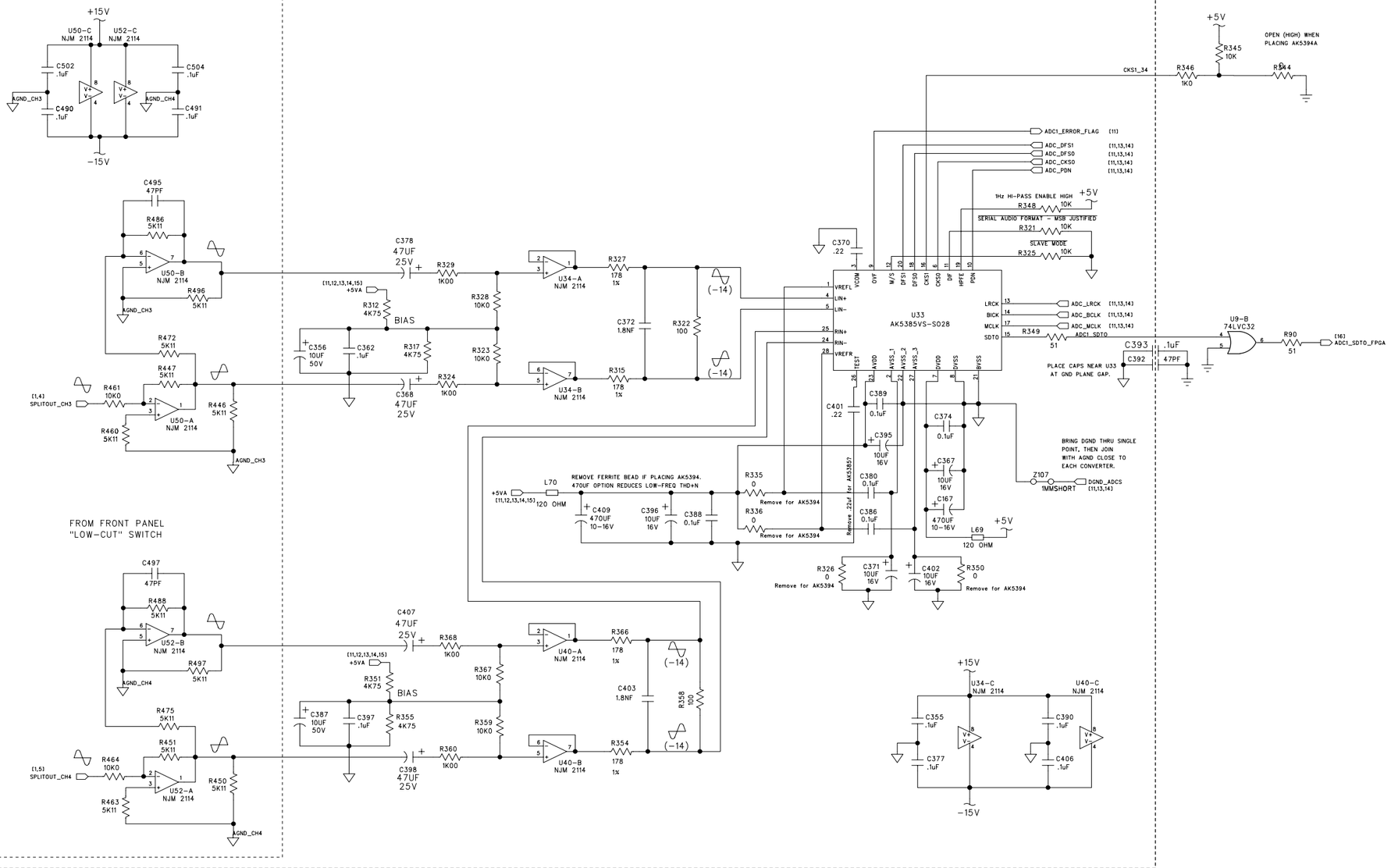
A-TO-D CHANNELS 3 & 4

PLACE OVER AGND PLANE

LOCATE ALONG CHANNELS

LOCATE ALONG AGND/DGND EDGE



PLACE OVER DGND PLANE

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ONYX 800R: MAIN			
SIZE: D	SCALE: NONE	DWG. NO. SCH0007715-00	REV. B00
DWG FILE:		SHEET 12 OF 18	

A-TO-D CHANNELS 5 & 6

PLACE OVER AGND PLANE

PLACE OVER DGND PLANE

LOCATE ALONG CHANNELS

LOCATE ALONG AGND/DGND EDGE

+15V
U54-C NJM 2114
U58-C NJM 2114
C506 .1uF
C550 .1uF
C492 .1uF
C539 .1uF
AGND_CH5
AGND_CH6
-15V

C499 47PF
R490 5K11
U54-B NJM 2114
R498 5K11
R478 5K11
R455 5K11
R467 10K0
{1,6} SPLITOUT_CH5
U54-A NJM 2114
R466 5K11
R454 5K11
AGND_CH5

C430 47UF 25V
R387 1K00
{11,12,13,14,15} +5VA
R373 4K75
BIAS
C417 10UF 50V
C419 .1uF
R378 4K75
C422 47UF 25V
R382 1K00
R386 10K0
R381 10K0
U44-A NJM 2114
U44-B NJM 2114
R385 178 1%
R375 178 1%
C426 1.8NF
R380 100
(-14)

FROM FRONT PANEL "LOW-CUT" SWITCH

C543 47PF
R575 5K11
U58-B NJM 2114
R585 5K11
R561 5K11
R538 5K11
R551 10K0
{1,7} SPLITOUT_CH6
U58-A NJM 2114
R537 5K11
R550 5K11
AGND_CH6

C448 47UF 25V
R404 1K00
{11,12,13,14,15} +5VA
R396 4K75
BIAS
C436 10UF 50V
C441 .1uF
R398 4K75
C444 47UF 25V
R401 1K00
R403 10K0
R400 10K0
U46-A NJM 2114
U46-B NJM 2114
R402 178 1%
R397 178 1%
C445 1.8NF
R399 100
(-14)

REMOVE FERRITE BEAD IF PLACING AK5394. 470UF OPTION REDUCES LOW-FREQ THD+N
+5VA {11,12,13,14,15}
L72 120 OHM
C446 470UF 10-16V
C439 10UF 16V
C434 0.1uF
R384 0 Remove for AK5394
R389 0 Remove for AK5394
C428 0.1uF
C433 0.1uF
Remove .22uf for AK5385?
C421 10UF 16V
R383 0 Remove for AK5394
C443 10UF 16V
R395 0 Remove for AK5394
C418 10UF 16V
C413 470UF 10-16V
L71 120 OHM
+5V

+15V
U44-C NJM 2114
U46-C NJM 2114
C416 .1uF
C429 .1uF
C437 .1uF
C447 .1uF
-15V

C420 .22
U43 AK5385VS-SO28
VCOM
VREFL
LIN+
LIN-
RIN+
RIN-
VREFR
OVF
M/S
DFS1
DFS0
CKS1
CKS0
DIF
HPFE
PDN
TEST
AVDD
AVSS_1
AVSS_2
AVSS_3
DVDD
DVSS
BVSS
C442 .22
C435 0.1uF
C440 10UF 16V
C425 0.1uF
BRING DGND THRU SINGLE POINT, THEN JOIN WITH AGND CLOSE TO EACH CONVERTER.
Z108 1MMSHORT
DGND_ADCS {11,12,14}

+5V
R391 10K
OPEN WHEN PLACING AK5394A
R390 0
CKS1_56
R392 1K0

ADC2_ERROR_FLAG {11}
ADC_DFS1 {11,12,14}
ADC_DFS0 {11,12,14}
ADC_CKS0 {11,12,14}
ADC_PDN {11,12,14}
1Hz HI-PASS ENABLE HIGH
R393 10K
SERIAL AUDIO FORMAT = MSB JUSTIFIED
R377 10K
SLAVE MODE
R379 10K
ADC_LRCK {11,12,14}
ADC_BCLK {11,12,14}
ADC_MCLK {11,12,14}
ADC2_SDTO {11,12,14}
R394 51
PLACE CAPS NEAR U43 AT GND PLANE GAP
C566 .1uF
C438 47PF
U9-C 74LVC32
R81 51
{16} ADC2_SDTO_FPGA

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SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715-00	B00
DWG FILE:		SHEET 13 OF 18	

A-TO-D CHANNELS 7 & 8

PLACE OVER AGND PLANE

PLACE OVER DGND PLANE

LOCATE ALONG CHANNELS

LOCATE ALONG AGND/DGND EDGE

+15V
U60-C NJM 2114
U62-C NJM 2114
C552 .1uF
C554 .1uF
C540 .1uF
C541 .1uF
AGND_CH7
AGND_CH8
-15V

+15V
U68-C NJM 2114
U69-C NJM 2114
C452 .1uF
C598 .1uF
C590 .1uF
C612 .1uF
-15V

C545 47PF
R577 5K11
U60-B NJM 2114
R586 5K11
AGND_CH7
R564 5K11
R542 5K11
{1,8} SPLITOUT_CH7
R554 10K0
U60-A NJM 2114
R541 5K11
R553 5K11
AGND_CH7

C591 47UF 25V
R622 1K00
{11,12,13,14,15} +5VA
R405 4K75
BIAS
C453 10UF 50V
C462 .1uF
R409 4K75
C463 47UF 25V
R413 1K00
R621 10K0
R412 10K0
U68-A NJM 2114
R620 178 1%
C467 1.8NF
R411 100
(-14)
U68-B NJM 2114
R407 178 1%
(-14)

FROM FRONT PANEL "LOW-CUT" SWITCH

C547 47PF
R579 5K11
U62-B NJM 2114
R587 5K11
AGND_CH8
R567 5K11
R546 5K11
{1,9} SPLITOUT_CH8
R557 10K0
U62-A NJM 2114
R545 5K11
R556 5K11
AGND_CH8

C613 47UF 25V
R643 1K00
{11,12,13,14,15} +5VA
R630 4K75
BIAS
C599 10UF 50V
C603 .1uF
R632 4K75
C604 47UF 25V
R636 1K00
R642 10K0
R635 10K0
U69-A NJM 2114
R640 178 1%
C609 1.8NF
R634 100
(-14)
U69-B NJM 2114
R631 178 1%
(-14)

C461 .22
U67 AK5385VS-S028
VCOM, OVF, M/S, DFS1, DFS0, CKS1, CKS0, DIF, HPFE, PDN
VREFL, LIN+, LIN-, RIN+, RIN-, VREFR
TEST, AVDD, AVSS_1, AVSS_2, AVSS_3, DVDD, DVSS, BVSS
C600 .22
C595 0.1uF
C597 10UF 16V
C460 0.1uF
C455 10UF 16V
C449 470UF 10-16V
C468 0.1uF
C593 0.1uF
C611 470UF 10-16V
C596 10UF 16V
C594 0.1uF
C458 10UF 16V
C601 10UF 16V
R625 0 Remove for AK5394
R410 0 Remove for AK5394
R619 0 Remove for AK5394
R623 0 Remove for AK5394
Remove 22uF for AK5385?
L85 120 OHM
L73 120 OHM
+5V
+5VA {11,12,13,14,15}

REMOVE FERRITE BEAD IF PLACING AK5394. 470UF OPTION REDUCES LOW-FREQ THD+N

ADC3_ERROR_FLAG {11}
ADC_DFS1 {11,12,13}
ADC_DFS0 {11,12,13}
ADC_CKS0 {11,12,13}
ADC_PDN {11,12,13}
1Hz HI-PASS ENABLE HIGH R626 10K
SERIAL AUDIO FORMAT - MSB JUSTIFIED R406 10K
SLAVE MODE R408 10K
LRCK, BICK, MCLK, SDTO
ADC_LRCK {11,12,13,14}
ADC_BCLK {11,12,13,14}
ADC_MCLK {11,12,13,14}
R627 51 ADC3_SDTO
U9-D 74LVC32
R94 51 {16} ADC3_SDTO_FPGA
C567 .1uF
C153 47PF
LOCATE CAPS NEAR SDTO NETS CROSSING GAP

+5V
R629 10K
OPEN (HIGH) WHEN PLACING AK5394A
CKS1_78
R624 1K0
R628 0

BRING DGND THRU SINGLE POINT, THEN JOIN WITH AGND CLOSE TO EACH CONVERTER.
Z109 1MMSHORT
DGND_ADCS {11,12,13,14}

PLACE THESE AC TERMINATIONS AT ENDS OF CLOCK LINES SHARED BETWEEN ADC'S.

{11,12,13,14} ADC_LRCK
{11,12,13,14} ADC_BCLK
{11,12,13,14} ADC_MCLK
DGND_ADCS {11,12,13,14}
C607 10pF R638 51
C606 10pF R637 51
C608 10pF R639 51
+5V
R646 100K
R645 100K
R647 100K
C568 .1uF
C22 47PF

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ONYX 800R: MAIN

SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715-00	B00
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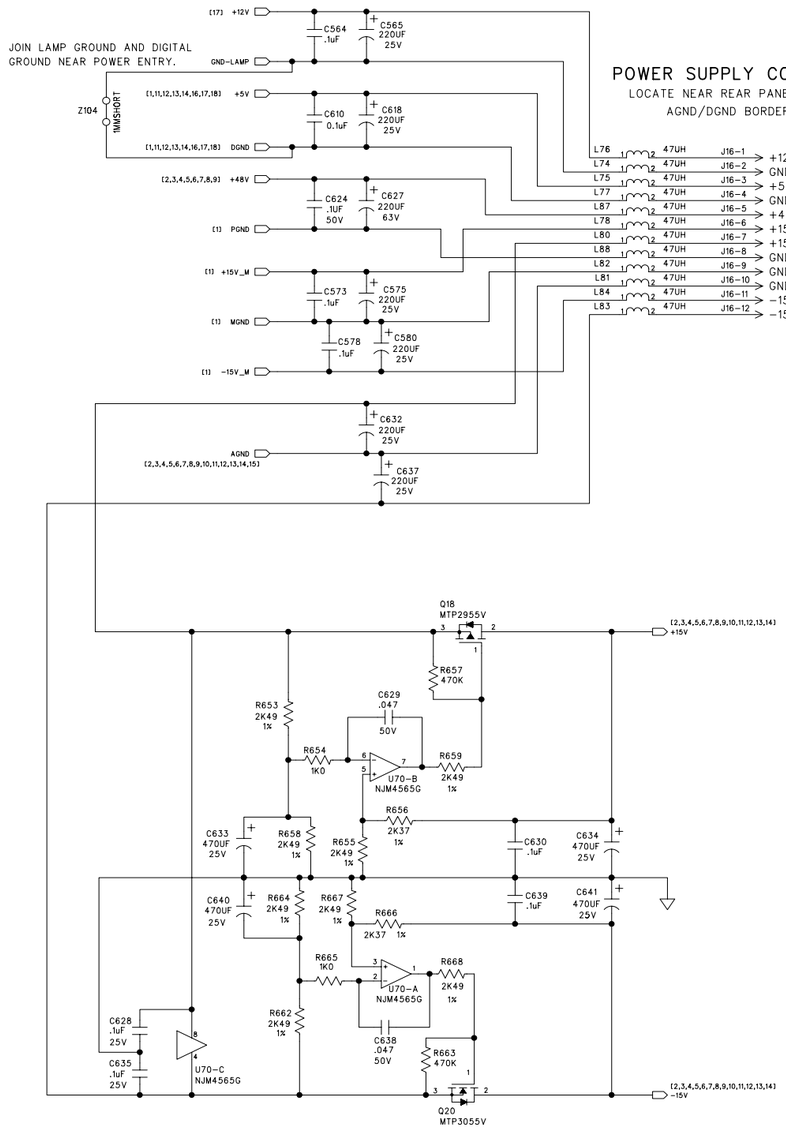
POWER ENTRY AND RESET

JOIN LAMP GROUND AND DIGITAL GROUND NEAR POWER ENTRY.



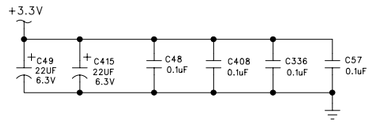
+/-15V POST REGULATION

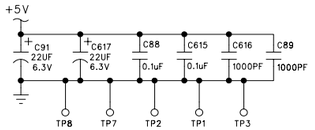
POWER SUPPLY CONNECTOR

LOCATE NEAR REAR PANEL ALONG AGND/DGND BORDER LINE.

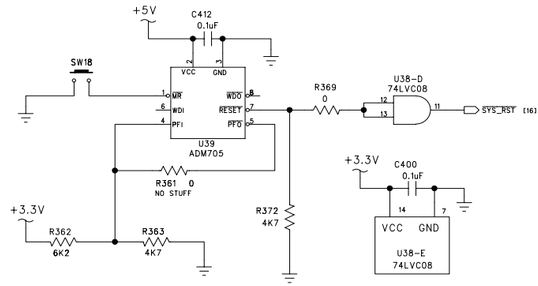
L76	47UH	J16-1	+12V-LL
L74	47UH	J16-2	GND-LAMP
L75	47UH	J16-3	+5V
L77	47UH	J16-4	GND-Digital
L87	47UH	J16-5	+48V
L78	47UH	J16-6	+15V-Meters
L80	47UH	J16-7	+15V-Analog
L88	47UH	J16-8	GND-48V
L82	47UH	J16-9	GND-Meters
L81	47UH	J16-10	GND-Analog
L84	47UH	J16-11	-15V-Meters
L83	47UH	J16-12	-15V-Analog

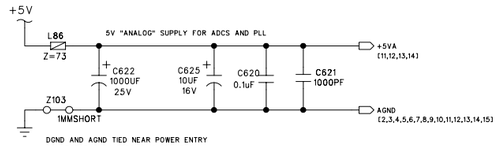
General decoupling and ground points spread evenly around digital section of board.

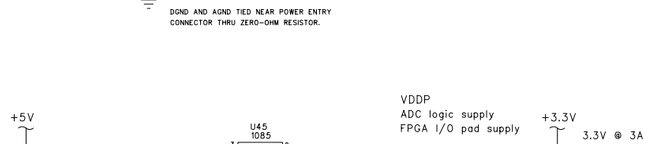


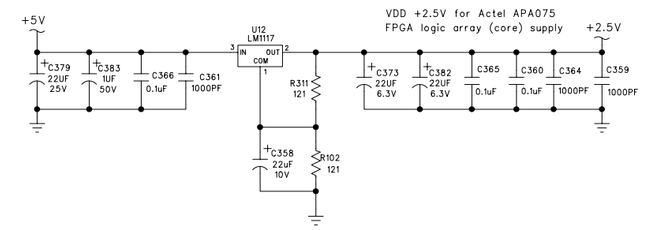


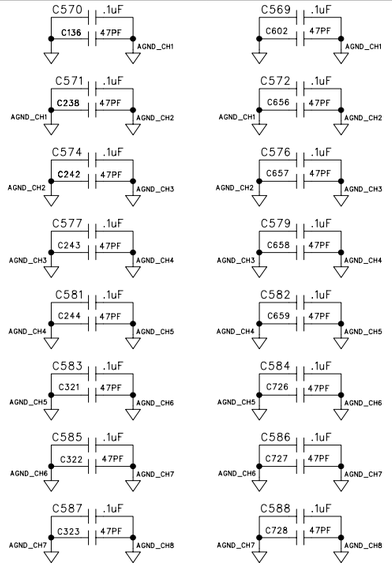
Reset



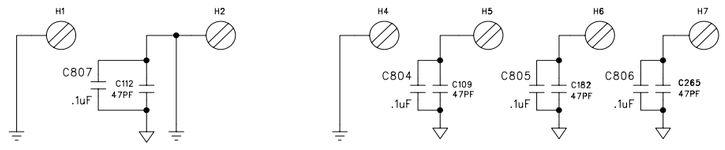




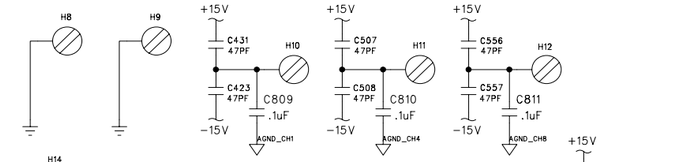




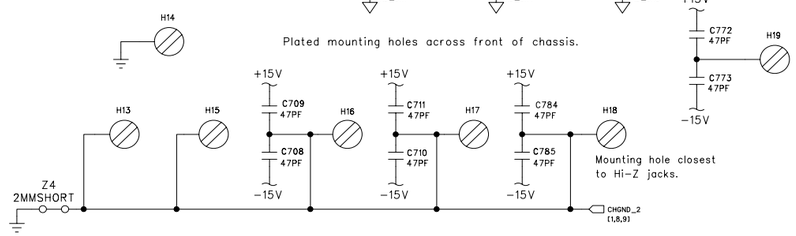
Plated mounting holes along back panel of chassis.



Plated mounting holes across middle of chassis.



Plated mounting holes across front of chassis.



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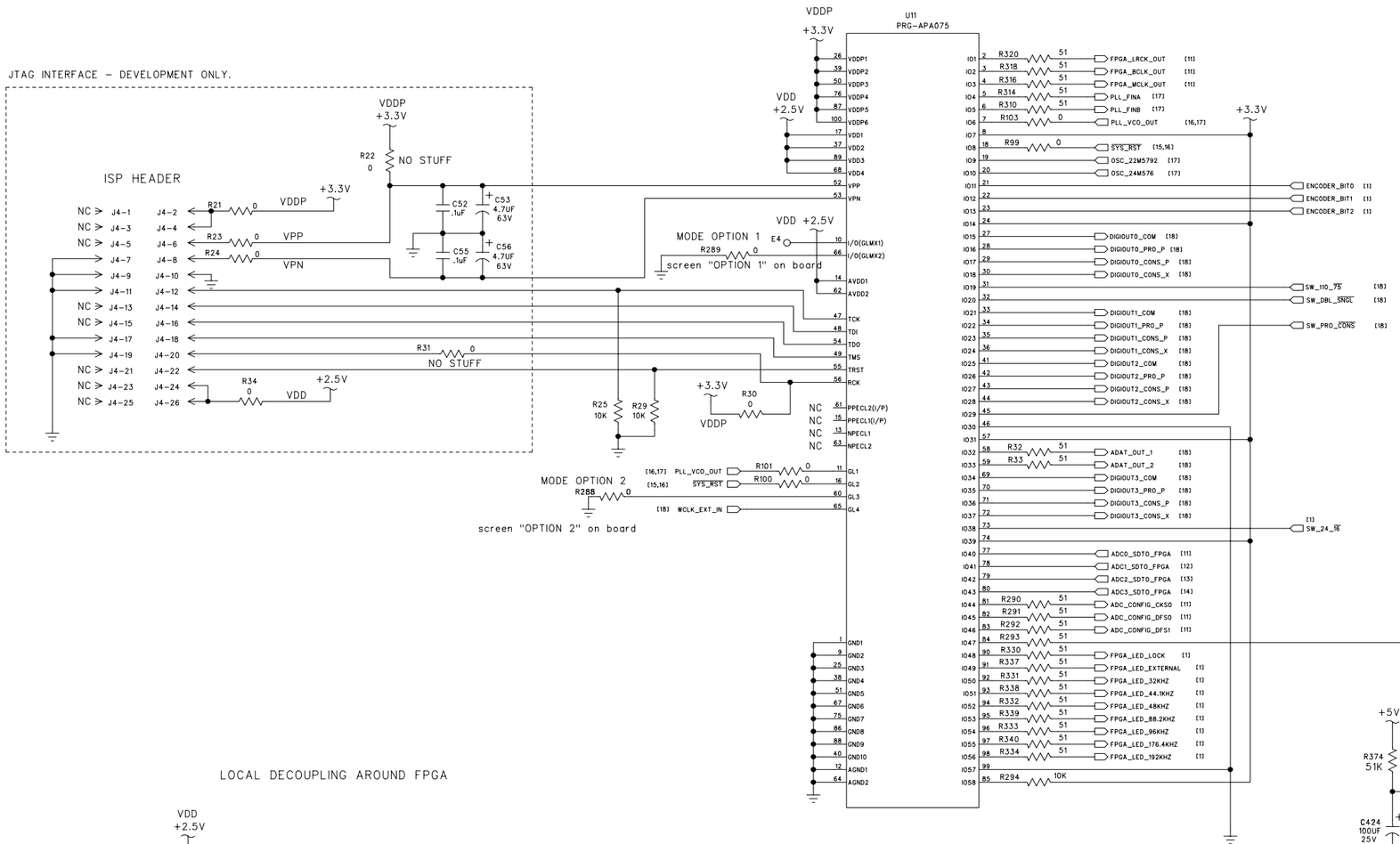
ONYX 800R: MAIN

SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715-00	B00
DWG FILE:		SHEET 15 OF 18	

FPGA

NOTE: FPGA pinout, footprint and ISP is compatible with
future next generation Actel ProASIC (see GCJ – details are under NDA)



Mackie Designs Inc. Woodinville, Wa.

ONYX 800R: MAIN

SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715-00	B00
DWG FILE:		SHEET 16 OF 18	

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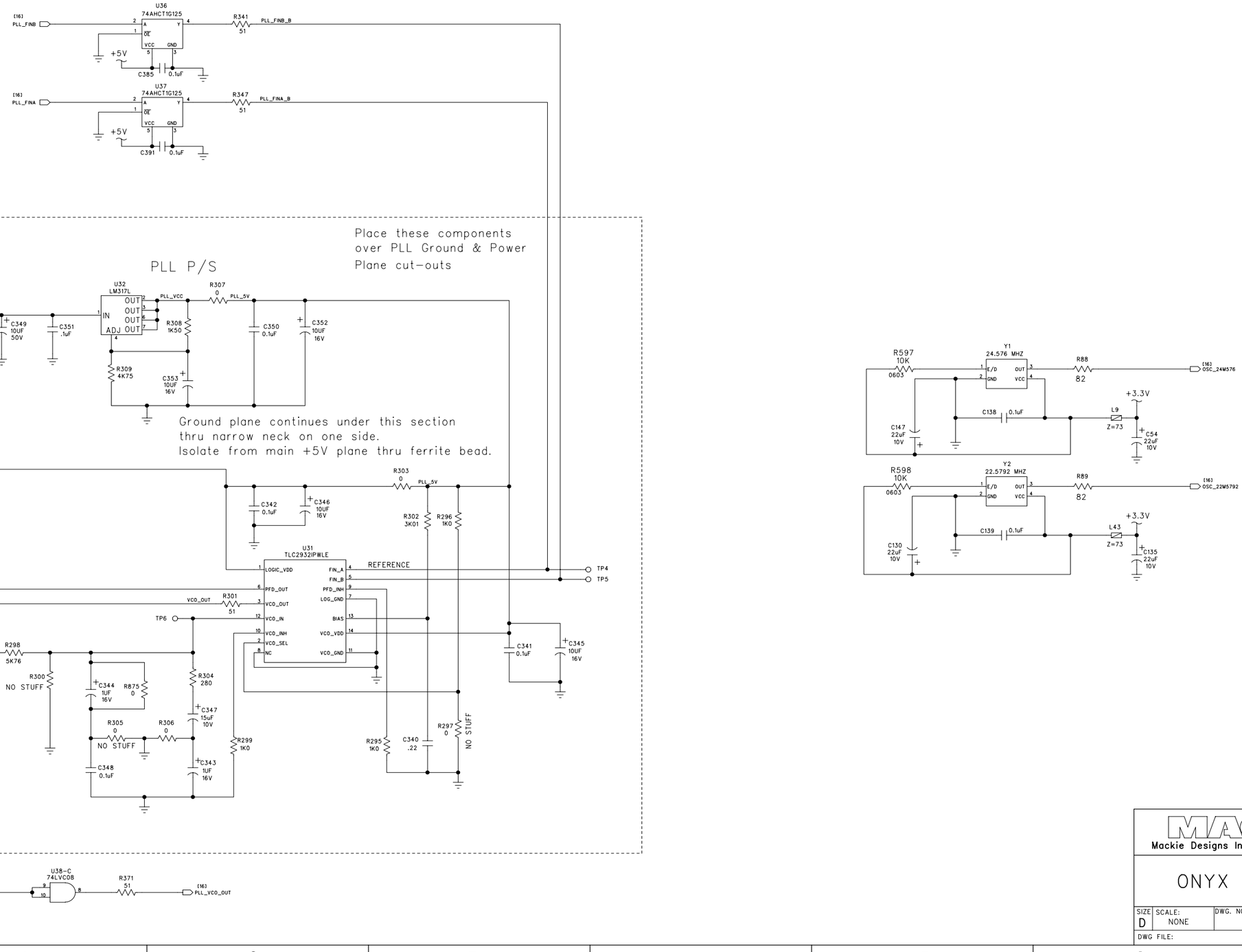
PLL AND CLOCKS



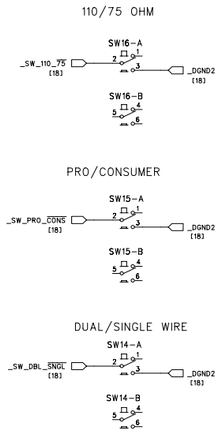
MACKIE.
Mackie Designs Inc. Woodinville, Wa.

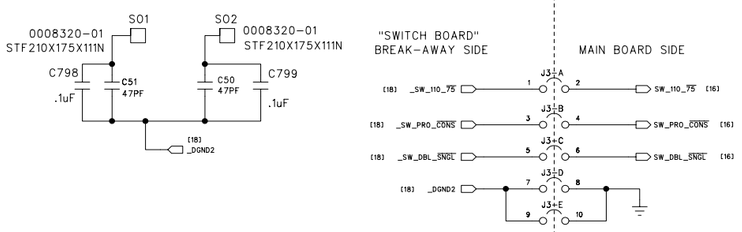
ONYX 800R: MAIN

SIZE	SCALE:	DWG. NO.	REV.
D	NONE	SCH0007715-00	B00
DWG FILE:		SHEET 17 OF 18	

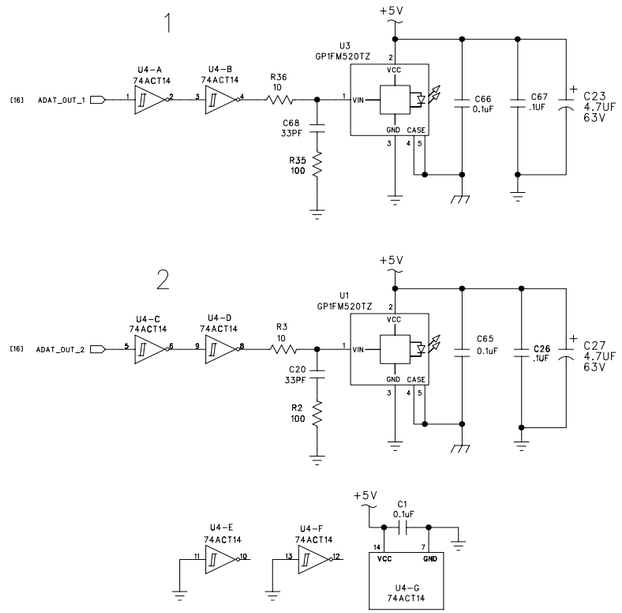
REAR PANEL DIGITAL I/O

SWITCH BOARD BREAK-AWAY FOR FORMAT SELECT SWITCHES

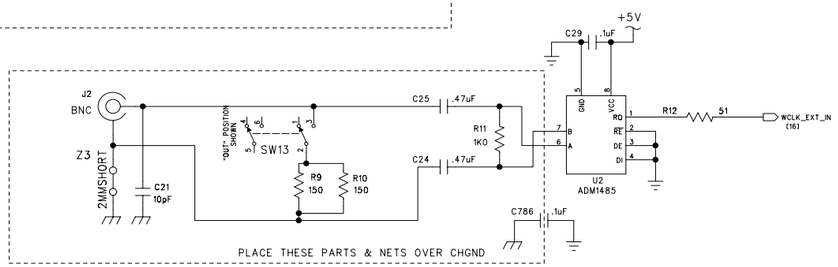




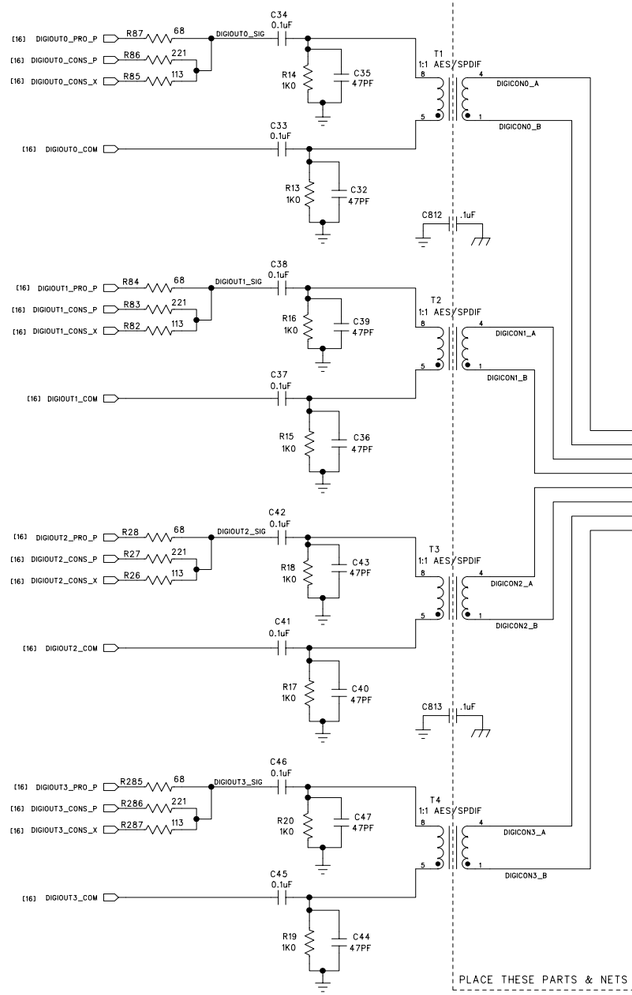
ADAT OPTICAL OUT



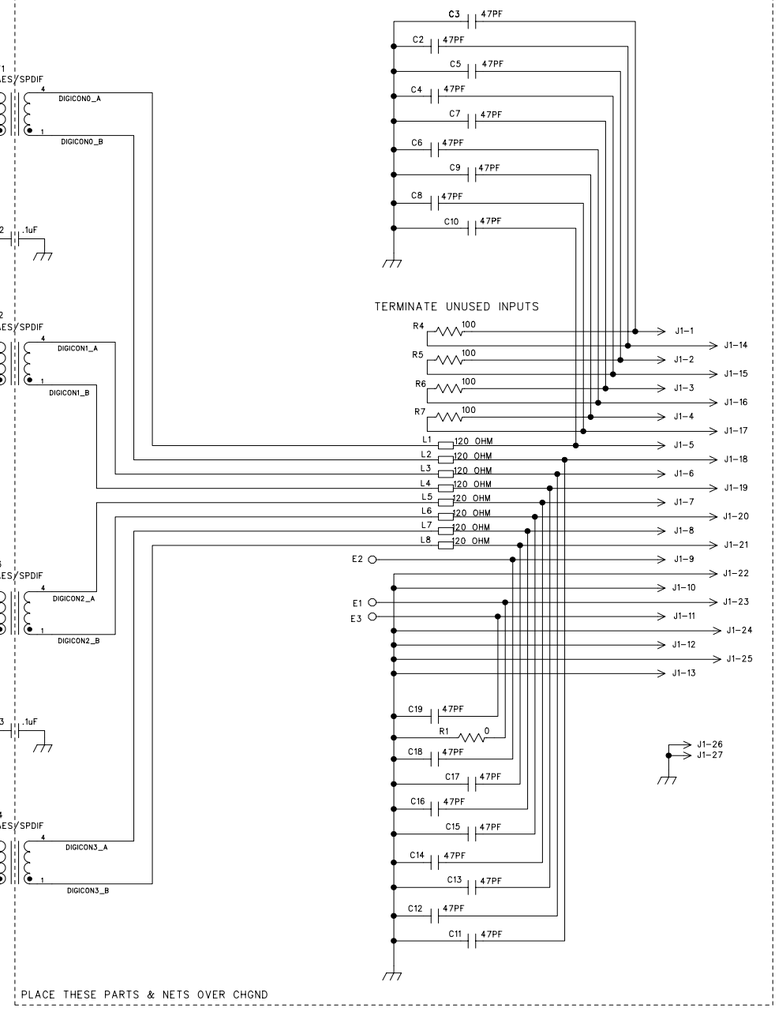
WORDCLOCK INPUT



LOCATE ISOLATION TRANSFORMERS AS CLOSE TO OUTPUT CONNECTOR "J1" AS POSSIBLE. TRANSFORMERS BRIDGE GAP BETWEEN DGND AND CHGND PLANE AREAS



AES3 or S/PDIF output DSUB-25



Z1 and Z2 short across gaps between planes near clock-like signals going across them.

MACKIE.
Mackie Designs Inc. Woodinville, Wa.

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D	NONE	SCH0007715-00	B00
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