

# COS/MOS INTEGRATED CIRCUIT

## PRELIMINARY DATA

### DUAL COMPLEMENTARY PAIR PLUS INVERTER

- QUIESCENT CURRENT SPECIFIED TO 15V (see page 10)
- MAX. INPUT LEAKAGE CURRENT  $1 \mu\text{A}$  @ 15V (FULL TEMP. RANGE)
- HIGH NOISE IMMUNITY: 45% of  $V_{DD}$  (TYP.)
- MEDIUM SPEED OPERATION:  $t_{PHL} = t_{PLH} = 50 \text{ ns}$  (TYP.) at  $C_L = 15 \text{ pF}$
- INPUTS FULLY PROTECTED
- LOW "1" and "0" OUTPUT LEVEL IMPEDANCE:  $500\Omega$  (TYP.) at  $V_{DD} - V_{SS} = 10\text{V}$
- HIGH FANOUT:  $> 50$

The **HBC 4007A** (extended temperature range) and **HBF 4007A** (standard temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.

They consist of three N-channel and P-channel enhancement-type MOS transistors. Each transistor is fully accessible to provide a convenient means for constructing the various typical circuits shown in figs. 13 to 19.

Typical applications are found in: extremely high-input impedance amplifiers, inverters, shapers, linear amplifiers, threshold detectors.

### ABSOLUTE MAXIMUM RATINGS

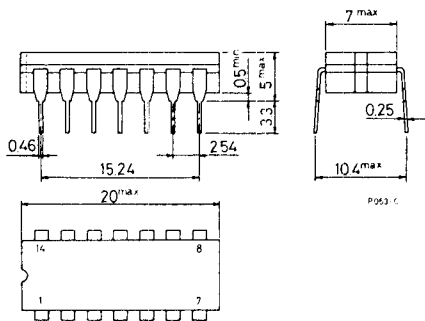
$V_{DD}-V_{SS}$	Supply voltage	-0.5 to 15	V
$V_i$	Input voltage (at any pin)	$V_{SS} \leq V_i \leq V_{DD}$	
$P_{tot}$	Total power dissipation (per package)	200	mW
$T_{stg}$	Storage temperature	-65 to 150	°C
$T_{op}$	Operating temperature: for <b>HBC</b> types	-55 to 125	°C
	for <b>HBF</b> types	-40 to 85	°C

### ORDERING NUMBERS:

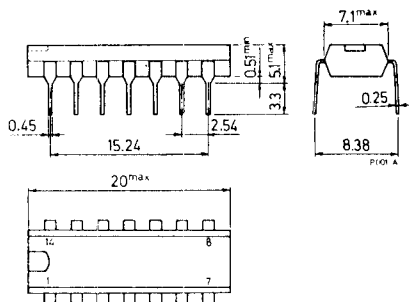
- HBC 4007 AD** for dual in-line ceramic package  
**HBC 4007 AF** for dual in-line ceramic package, frit seal (extended temperature range)  
**HBC 4007 AK** for ceramic flat package  
**HBF 4007 AE** for dual in-line plastic package  
**HBF 4007 AF** for dual in-line ceramic package, frit seal (standard temperature range)

## MECHANICAL DATA (dimensions in mm)

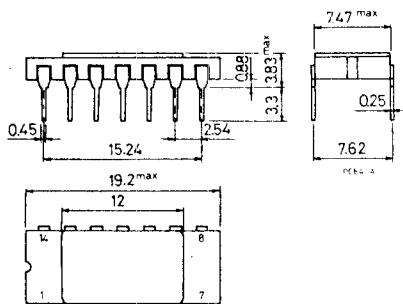
Dual in-line ceramic package  
for HBC/HBF 4007 AF



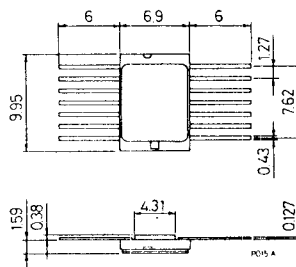
Dual in-line plastic package  
for HBF 4007 AE



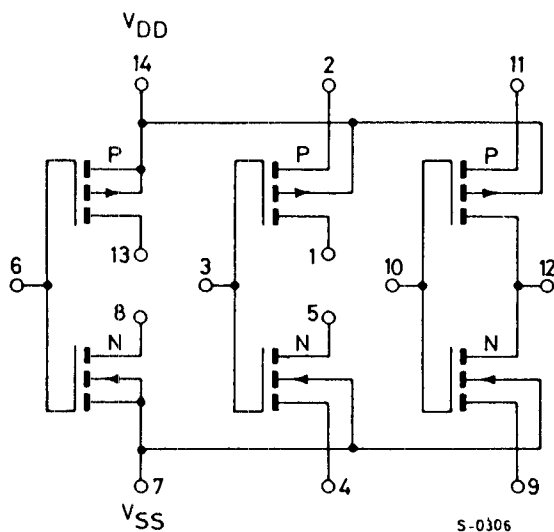
Dual in-line ceramic package  
for HBC 4007 AD



Ceramic flat package  
for HBC 4007 AK



## SCHEMATIC DIAGRAM



## RECOMMENDED OPERATING CONDITIONS

$V_{DD}^*$	Supply voltage	3 to 15	V
$V_I^*$	Input voltage	$V_{DD}$ to $V_{SS}$	
$T_{op}$	Operating temperature : for HBC types	-55 to 125	°C
	for HBF types	-40 to 85	°C

\* This is measured with respect to the  $V_{SS}$  pin voltage

**STATIC ELECTRICAL CHARACTERISTICS**

Parameter	Test conditions	Min.	Typ.	Max.	Unit
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**HBC types** (extended temperature range)

$I_L^*$	Quiescent current (for values at 15V see page 10)	$V_{DD} = 5V$ at $T_{amb} = -55^\circ C$ at $T_{amb} = 25^\circ C$ at $T_{amb} = 125^\circ C$  $V_{DD} = 10V$ at $T_{amb} = -55^\circ C$ at $T_{amb} = 25^\circ C$ at $T_{amb} = 125^\circ C$		0.05 0.001 0.05 3  0.1 0.001 0.1 6	$\mu A$ $\mu A$ $\mu A$  $\mu A$ $\mu A$ $\mu A$
$V_{OH}$	Output high voltage	$I_o = 0$ $V_{DD} = 5V$ at $T_{amb} = -55^\circ C$ at $T_{amb} = 25^\circ C$ at $T_{amb} = 125^\circ C$  $V_{DD} = 10V$ at $T_{amb} = -55^\circ C$ at $T_{amb} = 25^\circ C$ at $T_{amb} = 125^\circ C$	4.99 4.99 5 4.95  9.99 9.99 10 9.95		V V V  V V V
$V_{OL}$	Output low voltage	$I_o = 0$ $V_{DD} = 5V$ or $10V$ at $T_{amb} = -55^\circ C$ at $T_{amb} = 25^\circ C$ at $T_{amb} = 125^\circ C$	0.01 0 0.01 0.05		V V V
→ $V_{NH}$	Noise immunity	$V_{DD} = 5V$ $V_o = 0.95V$ at $T_{amb} = -55^\circ C$ at $T_{amb} = 25^\circ C$ at $T_{amb} = 125^\circ C$  $V_{DD} = 10V$ $V_o = 2.9V$ at $T_{amb} = -55^\circ C$ at $T_{amb} = 25^\circ C$ at $T_{amb} = 125^\circ C$	1.4 1.5 2.25 1.5  2.9 3 4.5 3		V V V  V V V

\* Obtained with test circuit of fig. 11

## STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{NL}$ Noise immunity	$V_{DD} = 5V$ $V_o = 3.6V$ at $T_{amb} = -55^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 125^{\circ}C$	1.5			V
		1.5	2.25		V
		1.4			V
	$V_{DD} = 10V$ $V_o = 7.2V$ at $T_{amb} = -55^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 125^{\circ}C$	3			V
		3	4.5		V
		2.9			V
					V
$I_{DN}$ Output drive current N-channel	$V_{DD} = 5V$ $V_o = 0.4V$ at $T_{amb} = -55^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 125^{\circ}C$	0.75			mA
		0.6	1		mA
		0.4			mA
	$V_{DD} = 10V$ $V_o = 0.5V$ at $T_{amb} = -55^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 125^{\circ}C$	1.6			mA
		1.3	2.5		mA
		0.95			mA
					mA
$I_{DP}$ Output drive current P-channel	$V_{DD} = 5V$ $V_o = 2.5V$ at $T_{amb} = -55^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 125^{\circ}C$	-1.75			mA
		-1.4	-4		mA
		-1			mA
	$V_{DD} = 10V$ $V_o = 9.5V$ at $T_{amb} = -55^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 125^{\circ}C$	-1.35			mA
		-1.1	-2.5		mA
		-0.75			mA
					mA
$I_{IH}, I_{IL}$ Input leakage current	$V_{DD} = 15V$ (any input)		$\pm 10^{-5}$	$\pm 1$	$\mu A$

## HBF types (standard temperature range)

$I_L^*$ Quiescent current (for values at 15V see page 10)	$V_{DD} = 5V$ at $T_{amb} = -40^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 85^{\circ}C$		0.5	$\mu A$
		0.005	0.5	$\mu A$
			15	$\mu A$
	$V_{DD} = 10V$ at $T_{amb} = -40^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 85^{\circ}C$		1	$\mu A$
		0.005	1	$\mu A$
			30	$\mu A$
				$\mu A$

**STATIC ELECTRICAL CHARACTERISTICS** (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{OH}$ Output high voltage	$I_o = 0$ $V_{DD} = 5V$ at $T_{amb} = -40^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 85^{\circ}C$ $V_{DD} = 10V$ at $T_{amb} = -40^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 85^{\circ}C$	4.99 4.99 4.95 9.99 9.99 9.95	5 10		V V V V V V
$V_{OL}$ Output low voltage	$I_o = 0$ $V_{DD} = 5V$ or $10V$ at $T_{amb} = -40^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 85^{\circ}C$			0.01 0 0.01 0.05	V V V
$V_{NH}$ Noise immunity	$V_{DD} = 5V$ $V_o = 0.95V$ at $T_{amb} = -40^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 85^{\circ}C$ $V_{DD} = 10V$ $V_o = 2.9V$ at $T_{amb} = -40^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 85^{\circ}C$	1.4 1.5 1.5 2.9 3 3	2.25	4.5	V V V V V V
$V_{NL}$ Noise immunity	$V_{DD} = 5V$ $V_o = 3.6V$ at $T_{amb} = -40^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 85^{\circ}C$ $V_{DD} = 10V$ $V_o = 7.2V$ at $T_{amb} = -40^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 85^{\circ}C$	1.5 1.5 1.4 3 3 2.9	2.25	4.5	V V V V V V
$I_{DN}$ Output drive current N-channel	$V_{DD} = 5V$ $V_o = 0.4V$ at $T_{amb} = -40^{\circ}C$ at $T_{amb} = 25^{\circ}C$ at $T_{amb} = 85^{\circ}C$	0.35 0.3 0.24	1		mA mA mA

# STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{D,N}$ Output drive current N-channel	$V_{DD} = 10V$ $V_o = 0.5V$ at $T_{amb} = -40^\circ C$ at $T_{amb} = 25^\circ C$ at $T_{amb} = 85^\circ C$	1.2 1 0.8	2.5		mA mA mA
$I_{D,P}$ Output drive current P-channel	$V_{DD} = 5V$ $V_o = 2.5V$ at $T_{amb} = -40^\circ C$ at $T_{amb} = 25^\circ C$ at $T_{amb} = 85^\circ C$  $V_{DD} = 10V$ $V_o = 9.5V$ at $T_{amb} = -40^\circ C$ at $T_{amb} = 25^\circ C$ at $T_{amb} = 85^\circ C$	-1.3 -1.1 -0.9  -0.65 -0.55 -0.45	-4		mA mA mA  mA mA mA
$I_{IH}, I_{IL}$ Input leakage current	$V_{DD} = 15V$ (any input)	$\pm 10^{-5}$	$\pm 1$		$\mu A$

\* Obtained with test circuit of fig. 11

Fig. 1 – Minimum and maximum voltage transfer characteristic curves and test circuit

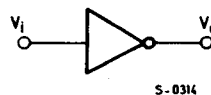
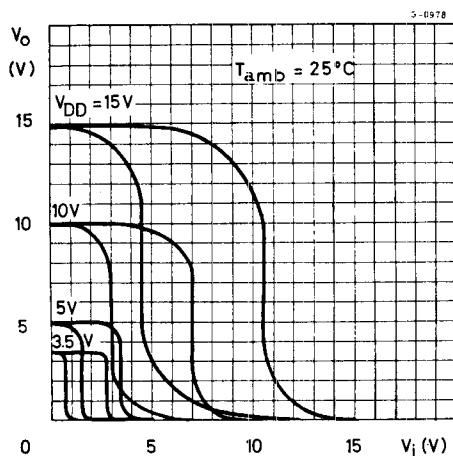


Fig. 2 - Typical voltage transfer characteristic curves and test circuit for NOR gate

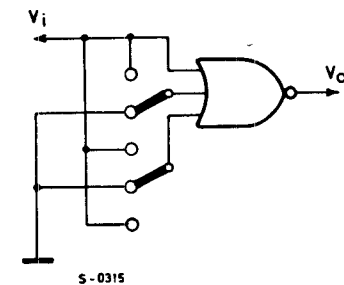
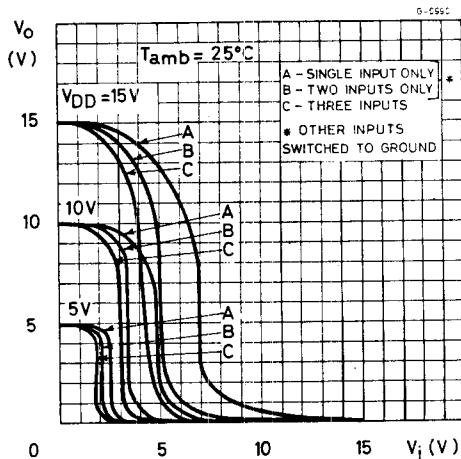
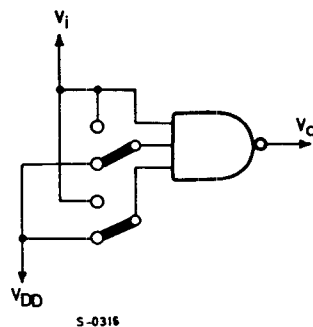
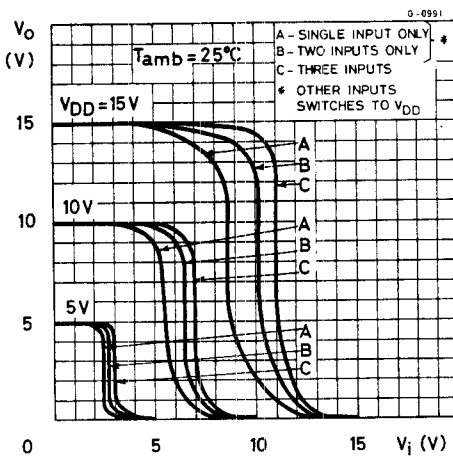
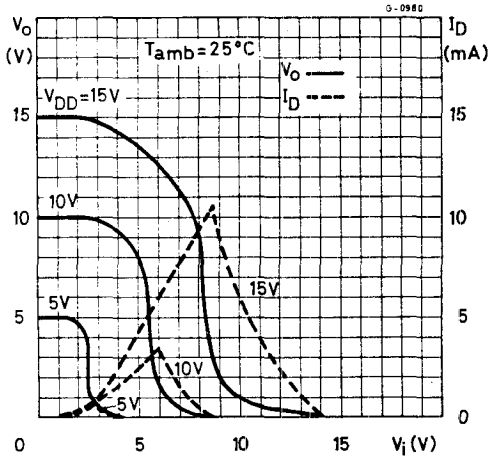


Fig. 3 - Typical voltage transfer characteristic curves and test circuit for NAND gate

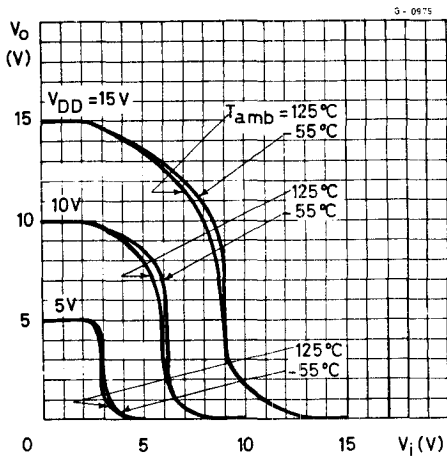




**Fig. 4 - Typical current and voltage transfer characteristic curves and test circuit for inverter**



**Fig. 5 - Typical voltage transfer characteristics versus ambient temperature**



**Fig. 6 - Typical power dissipation characteristics**

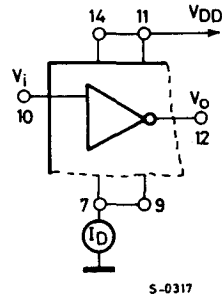


Fig. 7 - Typical N-channel drain characteristic curves and test circuit.

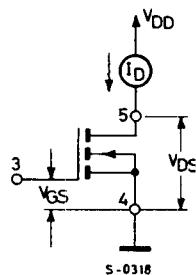
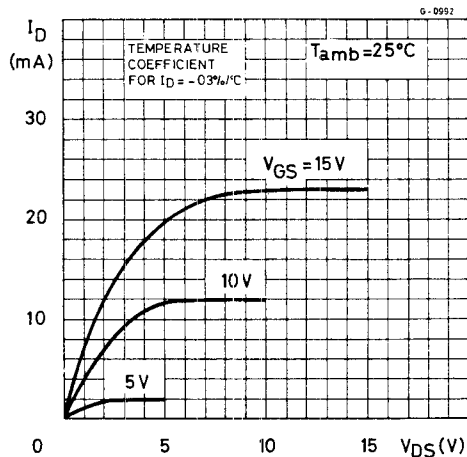
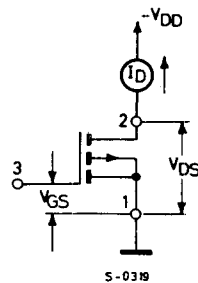
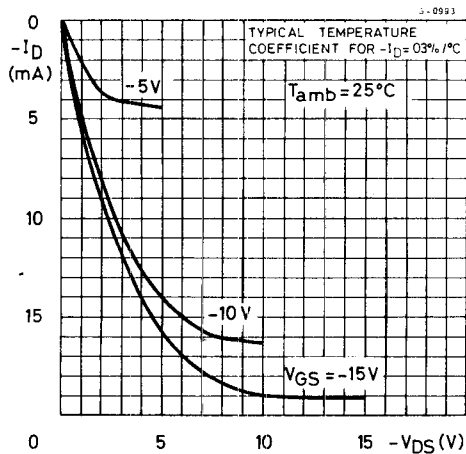
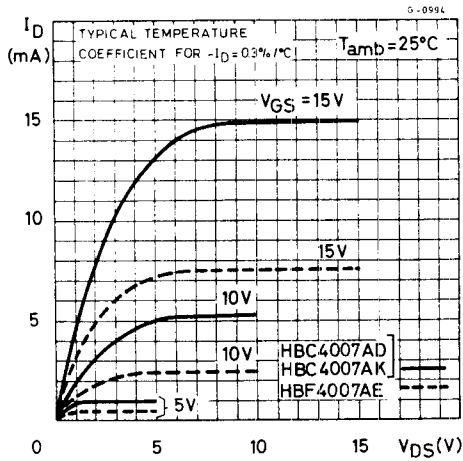


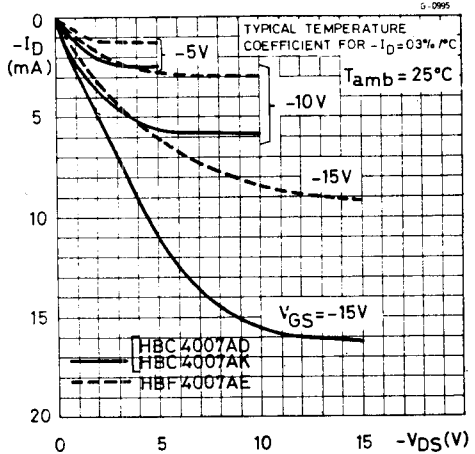
Fig. 8 - Typical P-channel drain characteristic curves and test circuit.



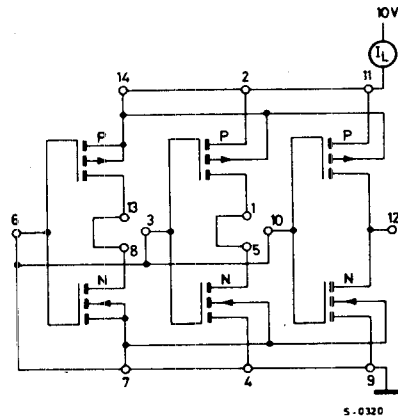
**Fig. 9 – Minimum N-channel drain characteristics**



**Fig. 10 – Minimum P-channel drain characteristics**



**Fig. 11– Quiescent device current test circuit**



**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$ ,  $C_L = 15 \text{ pF}$ , typical temperature coefficient for all  $V_{DD} = 0.3\%/^{\circ}\text{C}$  values)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{PLH}$ Propagation delay time (low to high level)	$V_{DD} = 5\text{V}$				
	for <b>HBC</b> types	35	60		ns
	for <b>HBF</b> types	35	75		ns
	$V_{DD} = 10\text{V}$				
	for <b>HBC</b> types	20	40		ns
	for <b>HBF</b> types	20	50		ns
$t_{PHL}$ Propagation delay time (high to low level)	$V_{DD} = 5\text{V}$				
	for <b>HBC</b> types	35	60		ns
	for <b>HBF</b> types	35	75		ns
	$V_{DD} = 10\text{V}$				
	for <b>HBC</b> types	20	40		ns
	for <b>HBF</b> types	20	50		ns
$t_{TLH}$ Transition time (low to high level)	$V_{DD} = 5\text{V}$				
	for <b>HBC</b> types	50	75		ns
	for <b>HBF</b> types	50	100		ns
	$V_{DD} = 10\text{V}$				
	for <b>HBC</b> types	30	40		ns
	for <b>HBF</b> types	30	50		ns
$t_{THL}$ Transition time (high to low level)	$V_{DD} = 5\text{V}$				
	for <b>HBC</b> types	50	75		ns
	for <b>HBF</b> types	50	100		ns
	$V_{DD} = 10\text{V}$				
	for <b>HBC</b> types	30	40		ns
	for <b>HBF</b> types	30	50		ns
$C_i$ Input capacitance	Any input for <b>HBC</b> and <b>HBF</b> types		5		pF

Fig. 12- Maximum propagation delay time versus  $V_{DD}$

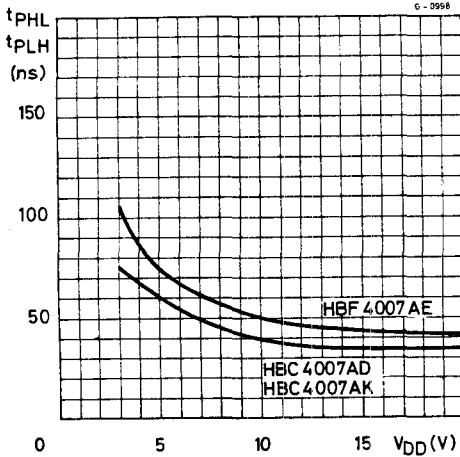
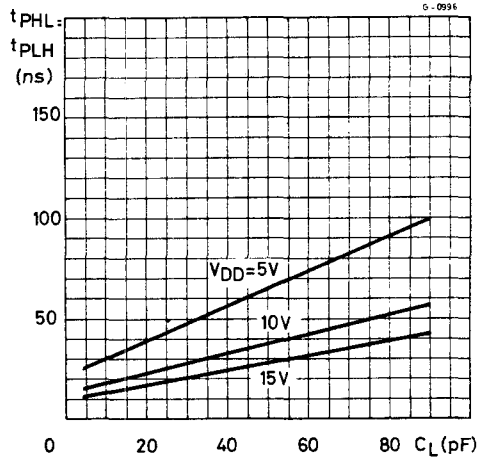


Fig. 13- Typical propagation delay time versus  $C_L$



## TYPICAL APPLICATIONS

Numbers shown in parentheses indicate pins that are connected together to form the various configurations listed.

Fig. 14- Triple inverters. (14, 2, 11); (8, 13); (1, 5); (4, 7, 9)

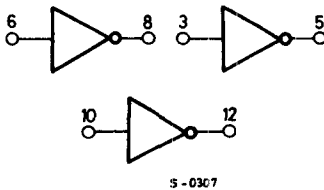


Fig. 15- 3-input NOR gate. (13, 2); (1, 11); (12, 5, 8); (7, 4, 9)

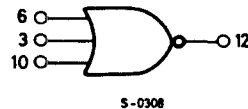


Fig. 16- 3-input NAND gate. (1, 12, 13); (2, 14, 11); (4, 8); (5, 9)

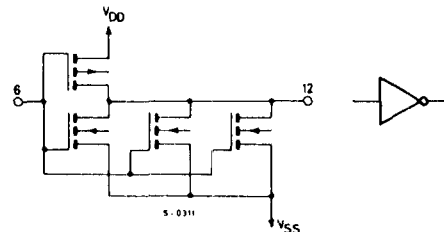
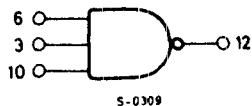


Fig. 18- High source-current driver. (6, 3, 10); (13, 1, 12); (14, 2, 11); (7, 9)

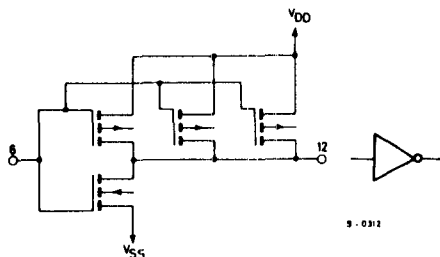


Fig. 19- High sink-and source-current driver. (6, 3, 10); (14, 2, 11); (7, 4, 9); (13, 8, 1, 5, 12)

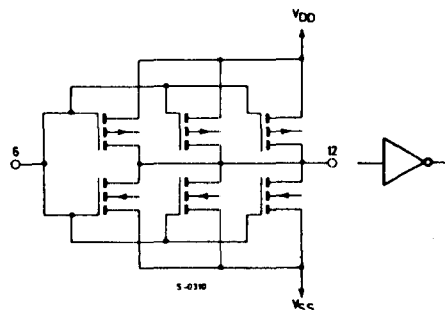


Fig. 20- Dual bi-directional transmission gating. (1, 5, 12); (2, 9); (11, 4); (8, 13, 10); (6, 3)

