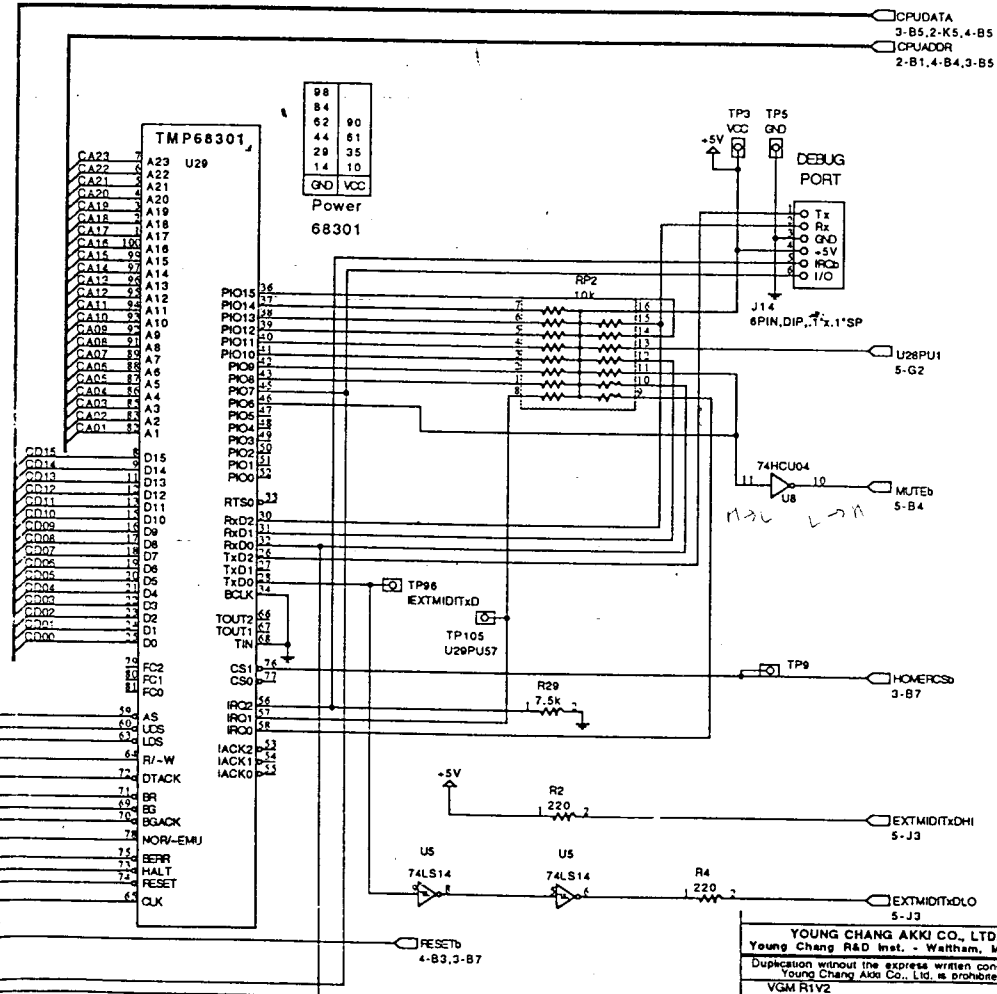


JP6 Jumper Legend
 1-2 -> TTL
 2-3 -> OPTO
 In silk screen add,
 "TTL" at pin 2,
 "OPTO" at pin 3.



NOTE: Signal names at TPxx
to appear in silk screen.

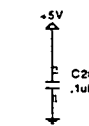
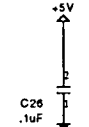
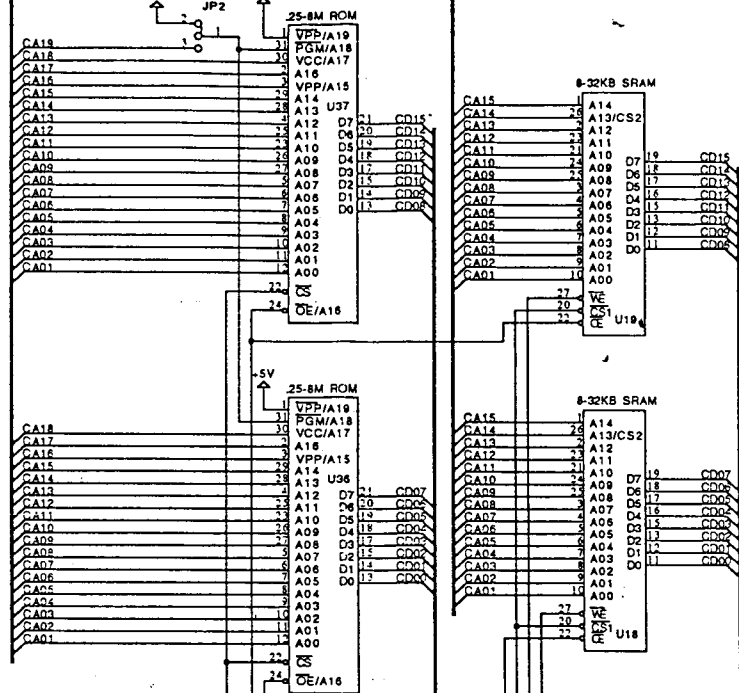
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 VGM R1V2
 683Q1
 Eng: Dairdre Hall By: _____
 Mfg: _____ SW 1 of 5
 Doc#: 011088 3/16/95 Rev: 1VER1

CPUAD0R
1-K2,4-B4,3-B5

JP2
Jumper Legend
1-2 -> 1 or 2 Meg
1-3 -> 4 or 8 Meg

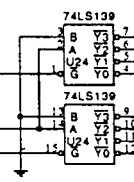
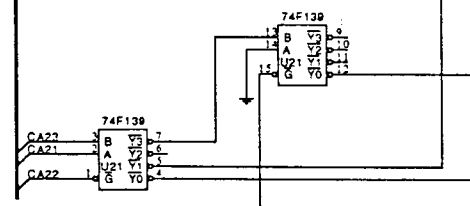
In silk screen add,
"1/2 Mb" at pin 2,
"4/8 Mb" at pin 3.

Eng /Setup EPROM
1/4 Meg



CPUADATA
1-K2,3-B5,4-B5

MARGEC5b
4-B3



CPUASb
1-B5

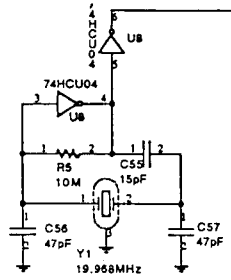
CPUUD5b
1-B6

CPURWb
1-B6,4-B3,3-B7

CPUUD5b
1-B6

NOTE: Signal names at TPxx
to appear in silk screen.

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VGM R1V2 CPU Memory	
Eng: Deirdre Hall	By:
Mfg:	Sht 2 of 5
Doc#: 011088	3/16/95 Rev: 1VER1



Homer
Power

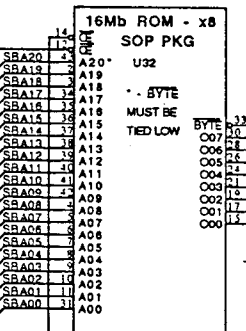
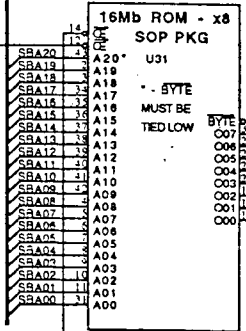
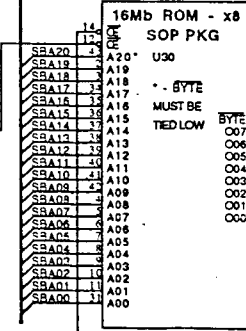
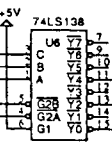
GND	VCC
8	5
14	12
15	13
23	22
24	28
38	37
44	45
48	46
49	50
69	71
70	72
91	89
92	90
104	106
105	107
115	117
116	118

Homer

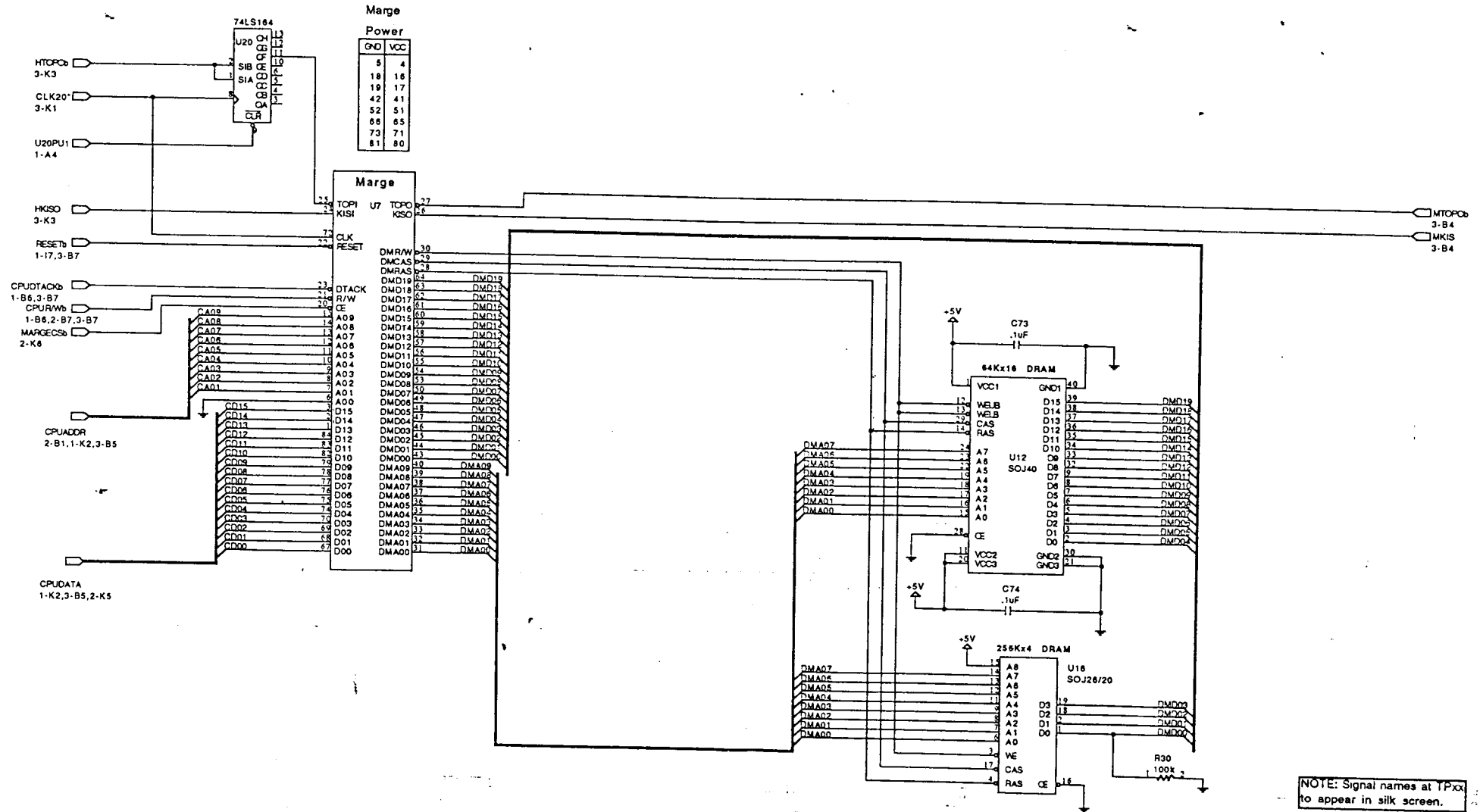
U4	U4
KIS1	KIS1
Y00	Y00
SMA23	SBA23
SMA22	SBA22
SMA21	SBA21
SMA20	SBA20
SMA19	SBA19
SMA18	SBA18
SMA17	SBA17
SMA16	SBA16
SMA15	SBA15
SMA14	SBA14
SMA13	SBA13
SMA12	SBA12
SMA11	SBA11
SMA10	SBA10
SMA09	SBA09
SMA08	SBA08
SMA07	SBA07
SMA06	SBA06
SMA05	SBA05
SMA04	SBA04
SMA03	SBA03
SMA02	SBA02
SMA01	SBA01
SMA00	SBA00
SMD11	SBD11
SMD10	SBD10
SMD09	SBD09
SMD08	SBD08
SMD07	SBD07
SMD06	SBD06
SMD05	SBD05
SMD04	SBD04
SMD03	SBD03
SMD02	SBD02
SMD01	SBD01
SMD00	SBD00
SMRAS/A5	SBRAS/A5
SMRUX	SBRUX
SMCAS/OE	SBCAS/OE
SMAS	SBRAS
DAC0	DAC0
DAC1	DAC1
DIE2	DIE2
DIE1	DIE1
DIE3	DIE3
DIE4	DIE4
DLE1	DLE1
DLE0	DLE0
HOSTA	HOSTA
OSR7	OSR7
OSR11	OSR11
OSR10	OSR10

CA11	BUSA11
CA10	BUSA10
CA09	BUSA09
CA08	BUSA08
CA07	BUSA07
CA06	BUSA06
CA05	BUSA05
CA04	BUSA04
CA03	BUSA03
CA02	BUSA02
CA01	BUSA01
CA00	BUSA00
CD14	BUSD14
CD13	BUSD13
CD12	BUSD12
CD11	BUSD11
CD10	BUSD10
CD09	BUSD09
CD08	BUSD08
CD07	BUSD07
CD06	BUSD06
CD05	BUSD05
CD04	BUSD04
CD03	BUSD03
CD02	BUSD02
CD01	BUSD01
CD00	BUSD00

CPUDOR	2-B1,1-K2,4-B4
CPUDATA	1-K2,2-K5,4-B5
HOMERSD	1-K8
CPURWb	1-B6,2-B7,4-B3
CPUDACK	1-B6,4-B3
RESETb	1-17,4-B3



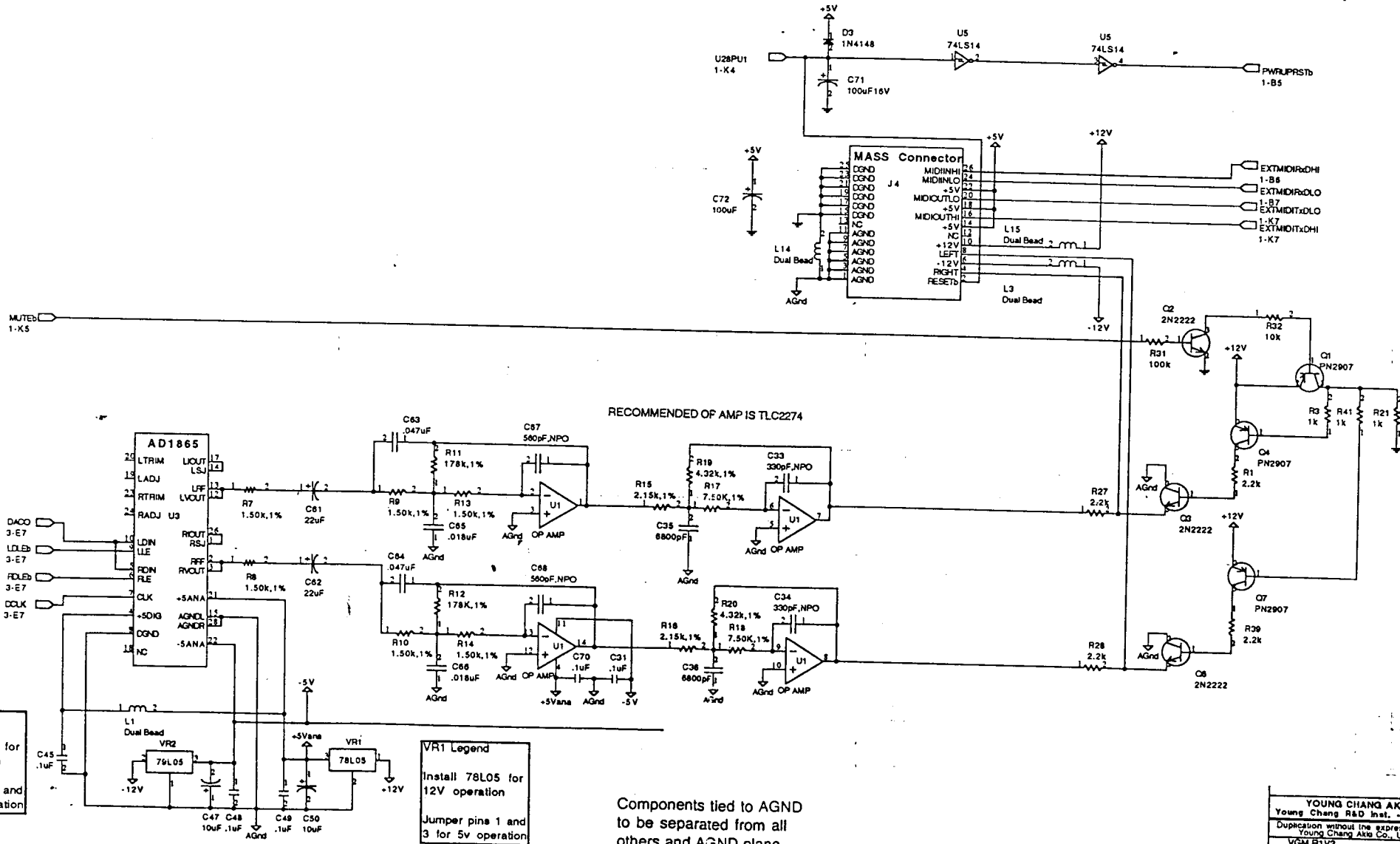
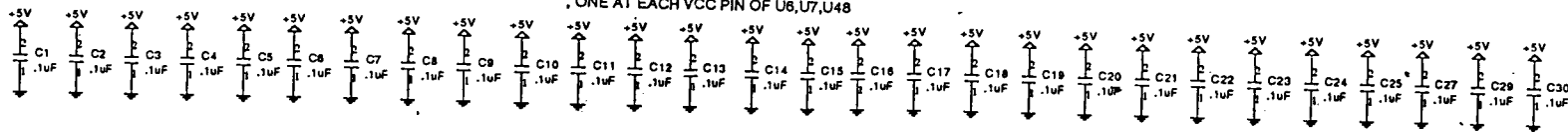
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VGM-R1V2
Homer
Eng: Deirdre Hall By: _____
Mfg: _____ Sht 3 of 5
Doc#: 011088 3/16/95 Rev: 1VER1



NOTE: Signal names at TPxx to appear in silk screen.

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 VGM R1V2
 Marge w Delay RAM
 Eng: Deirdre Hall By:
 Mfg: Sh 4 of 5
 Doc#: 011088 3/16/95 Rev. 1VER1

DECOUPLING CAPS, ONE AT EACH GROUND PIN OF U1,U2,U5,U8,U12,U16-U21,U28-U32
 , ONE AT EACH VCC PIN OF U6,U7,U48



RECOMMENDED OP AMP IS TLC2274

VR2 Legend
 Install 79L05 for 12V operation
 Jumper pins 2 and 3 for 5v operation

VR1 Legend
 Install 78L05 for 12V operation
 Jumper pins 1 and 3 for 5v operation

Components tied to AGND to be separated from all others and AGND plane separated from DGND plane.

NOTE: Signal names at TPxx to appear in silk screen.

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 DAC w/ filter and amp. Battery/Reset. Misc.
 Eng. Deirdre Hall By: _____
 Mfg: _____ SM 5 of 5
 Doc#: 011088 3/16/95 Rev. 1VER1