



DESIGNATOR	DESCRIPTION	SLM PART #
D1	LED, RED-GREEN	21-991-51
D2-D5	1N4002	21A402-01
D6, 7	1N754	21A754-01
D8-D17	1N914	21A914-01
D18	1N4743	21A443-01
D19	1N914	21A914-01
IC1-IC5, IC7	TLO72	37-072-01
IC6	NE532	37-532-01
J1	2 PIN HEADER	17-311-02
J2	8 PIN HEADER	17-311-08
J3	1/4" JACK	39-012-01
P1-P7	20K POT (SLIDER)	70-203-51
Q1	J176	96-176-01
Q2	J112	96-112-01
Q3	2N5210	96-510-01
R46	1/4W THERMISTOR	73-101-01

TEST POINTS	VOLTAGE V p-p	VOLTAGE VDC
1	.5	0
2	.5	0
3	.5	0
4	.5 EQ OFF	0
	.39 EQ ON	0
5	.5	0
6	.5	0
7	.23	0
8	.23	0
9	---	+15
10	---	+6.8
11	---	-15
12	---	-6.8
13	---	-14
14	W/ 3 & TP1	+14
	---	-14 (GND)
	---	+14 (STANDBY)

CONDITIONS:
 VOLTAGES ARE MEASURED WITH ALL POTS & CONTROL POSITION. FRONT PANEL EQ ENABLED (L2-7 & GND) & BALANCED OUT SLEW BY.
 INPUT: 100mV SINE WAVE @ 500Hz EQ TO GND (L2-5).

- NOTES**
- 1) THIS UNIT CONTAINS HAZARDOUS VOLTAGE. DISCONNECT POWER AND BE SURE POWER SUPPLY IS DISCHARGED BEFORE TOUCHING INTERNAL PARTS.
 - 2) UNLESS NOTED, RESISTOR VALUES IN OHMS, 1/4W-5% TOL. CAPACITOR VALUES IN MICROFARADS, 50V-10% TOL.
 - 3) VOLTAGES ARE MEASURED WITH 1 MEGOHM OSCILLOSCOPE AND 10 MEGOHM DIGITAL VOLTMETER.
 - 4) CIRCUIT GROUND /// SWITCHED GROUND ∇ CHASSIS GROUND \oplus

REV	DATE	BY	CHKD	DESCRIPTION
3	3/10/82	SMR		REVISION
2	11/1/81	SMR		CHANGED VALUE OF CAPACITORS, CHANGES IN RES. AND RES.
1	12/4/80	ML		REDRAWN DUE TO CIRCUIT CHANGES

SIGNATURES:	DATE:	1980 BORGWALD DR. ST. LOUIS, MISSOURI 63104
CHKD: MGA	7-19-83	
APPD:		
ISSUED:		
PROJECT NAME:	SVT-II GRAPHIC EQ	
PLOT DATE:	04/29/82	DRAWING NO. SCHEMATIC
PLOT TIME:	12:43:54	DRAWING NO. 075728-01
FILE NAME:	73728013	