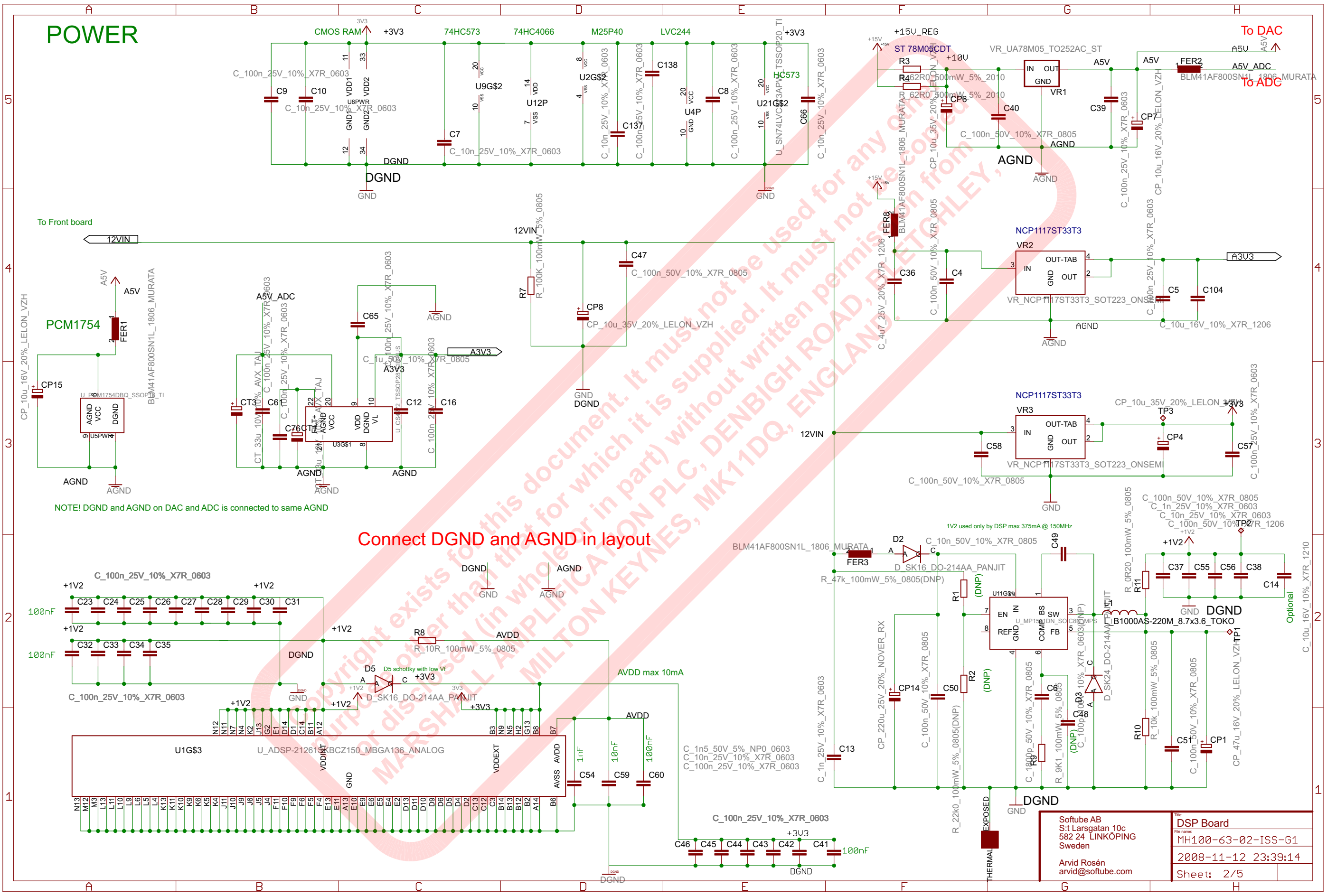


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INFO1
used lib: DSP_90 ver 20080407

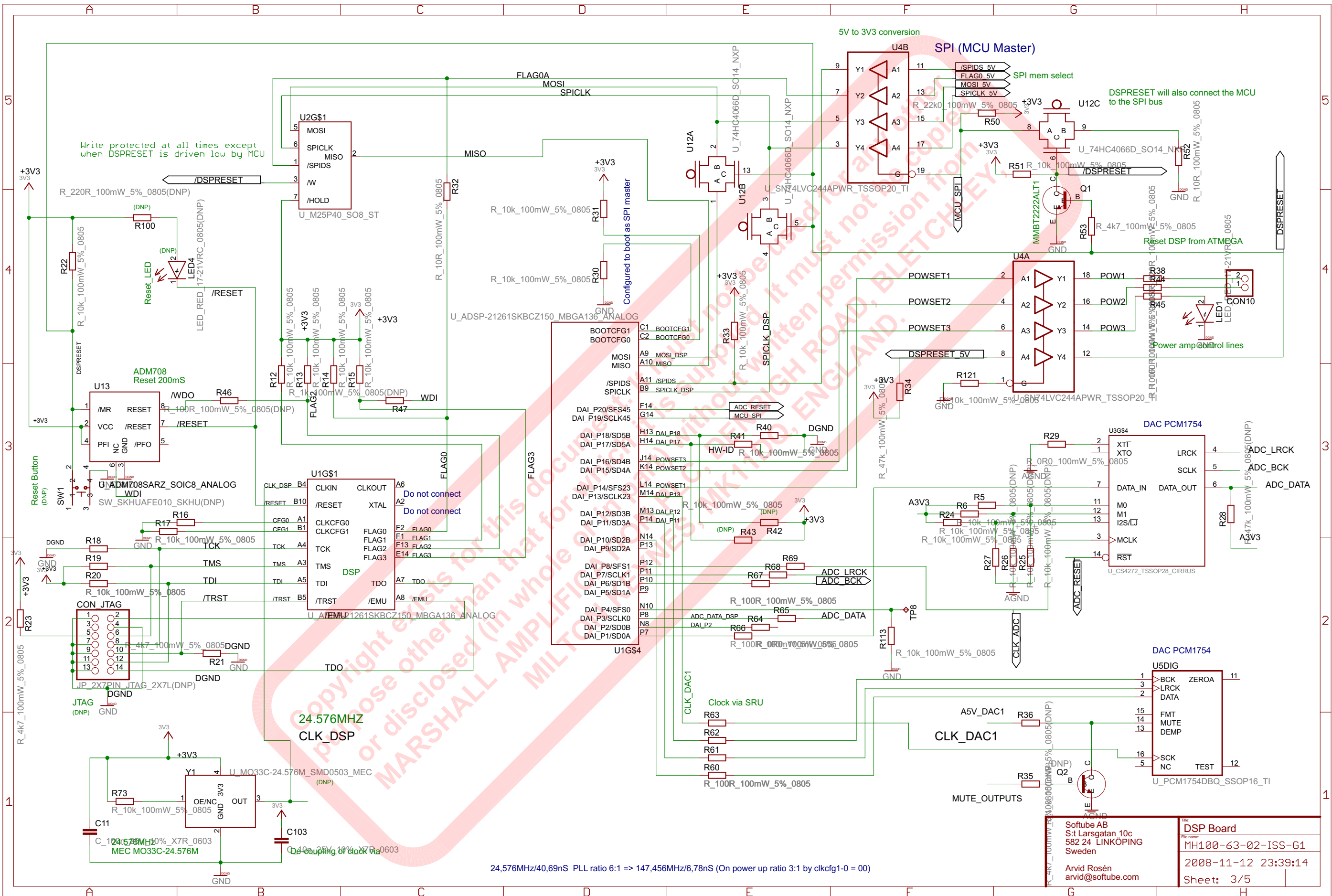
POWER



Connect DGND and AGND in layout

NOTE! DGND and AGND on DAC and ADC is connected to same AGND

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Write protected at all times except when DSPRESET is driven low by MCU

Configured to boot as SPI master

5V to 3V3 conversion

SPI (MCU Master)

DSPRESET will also connect the MCU to the SPI bus

Reset DSP from ATMEGA

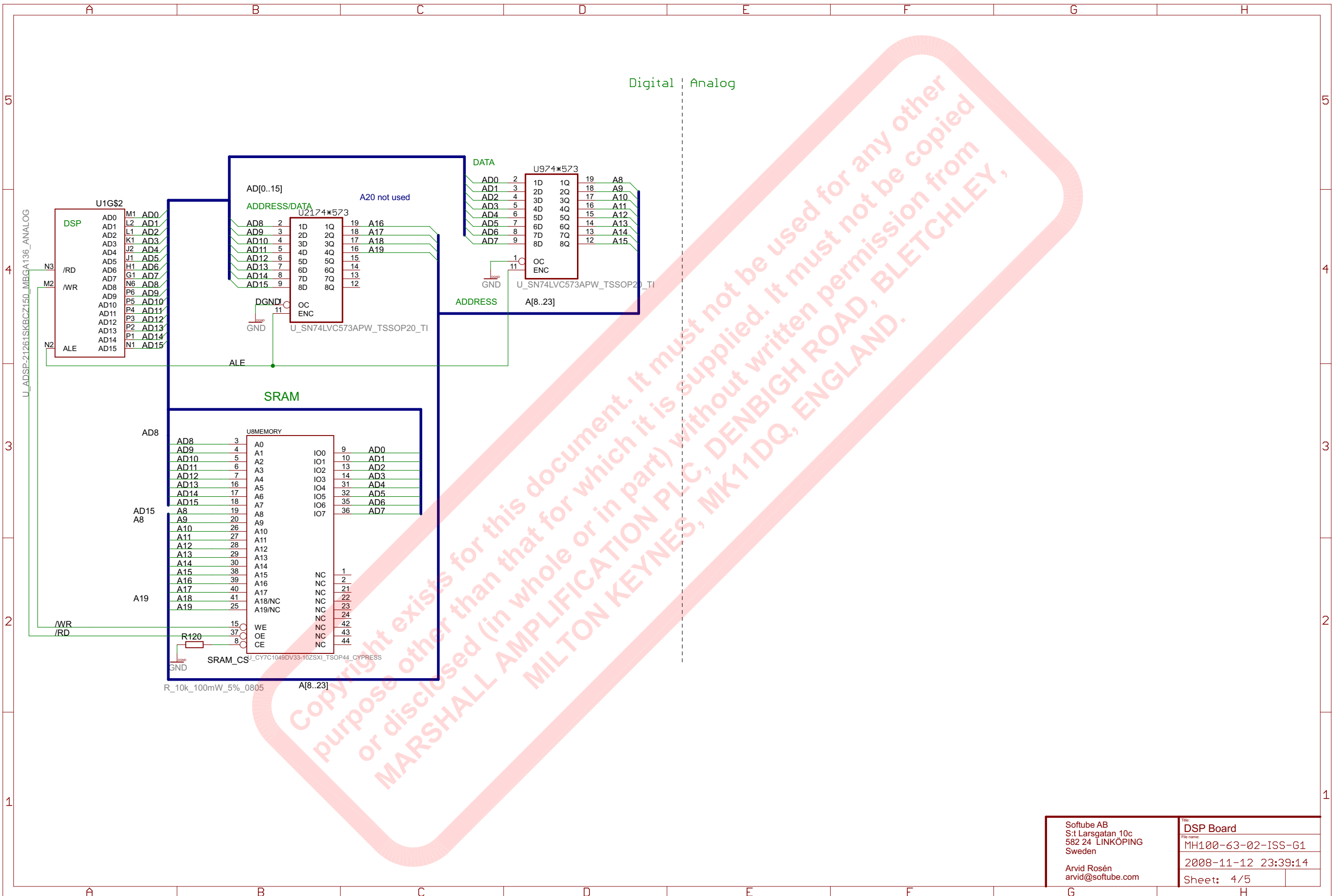
Power amp control lines

24.576MHZ
CLK_DSP

24,576MHz/40,69nS PLL ratio 6:1 => 147,456MHz/6,78nS (On power up ratio 3:1 by clkcfg1-0 = 00)

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