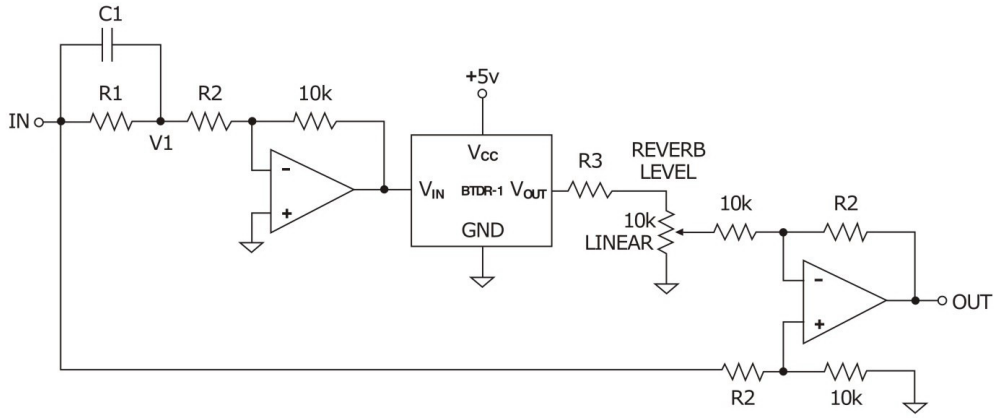
Application Circuit



- The value of R2 sets the proper input level to the BTDR-1. Set R2=6.7kΩ · V_1, where V_1 is the maximum peak voltage measured at node V_1 shown in the schematic above.
- C1 and R1 are optional and create a high-pass or shelf filter that attenuates the low frequency input to the reverb.
  - For a low shelf filter:
    - Set C1 = $1/(2\pi \cdot R2 \cdot f_c)$, where f_c is the shelf frequency.
    - Set R1 = $R2 \cdot (1-G_s) / G_s$, where G_s is the shelf gain.
  - For a high-pass filter:
    - Set C1 = $1/(2\pi \cdot R2 \cdot f_c)$, where f_c is the cutoff frequency.
    - Omit R1 (R1 = 0)
- Adjust R3 to limit maximum reverb level. R3 may be omitted for maximum reverb level.
- The use of a regulated 5V supply, such as a 78L05, is highly recommended. A ceramic bypass capacitor may be necessary between V_{cc} and GND if the regulator is not close to the reverb module.
- Audio noise during power-down can be minimized by quickly discharging supply from 5V to 0V; otherwise, external output muting is recommended.

Example:

Configure the circuit above for a shelf filter with f_c= 200 Hz and 10 dB attenuation when the Maximum voltage at V_1 =8V_{PK}.

- R2=6.7kΩ · 8V=53.6kΩ
- C1=1/(2π · 53.6kΩ · 200Hz) ≈ 0.015μF
- $G_s = 10^{(-10dB)/20} = 0.316$
- R1 = 53.6kΩ · (1-0.316)/0.316 ≈ 115kΩ

Considerations for FCC Compliance

- No high-frequency clocks are conducted outside of BTDR-1's internal ICs, minimizing emissions.
- Use of the BTDR-1V (vertical mounting) should lower conducted emissions, since it eliminates parallel signal paths between the BTDR-1 and main interface PC board.
- No guarantees of FCC compliance are made for the BTDR-1,as it has not been tested for radio-frequency emissions, either radiated or conducted.

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