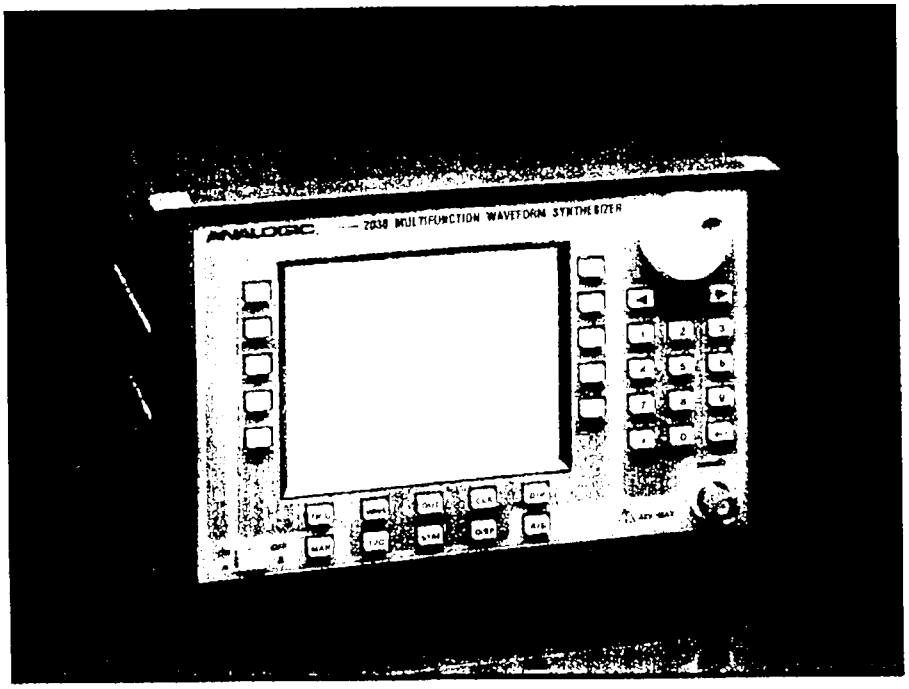
Model 2030

MULTIFUNCTION WAVEFORM SYNTHESIZER



H A R D W A R E

MAINTENANCE MANUAL

ANALOGIC

The World Resource for Precision Signal Technology

MODEL 2030

Multifunction Waveform Synthesizer

ANALOGIC®

The World Resource for Precision Signal Technology

Proprietary Statement

The information contained in this publication is derived in part from proprietary and patent data of the Analogic Corporation. This information has been prepared for the express purpose of assisting operating and maintenance personnel in the efficient use of the instrument described herein. Publication of this information does not convey any rights to reproduce it or to use it for any purpose other than in connection with the installation, operation, and maintenance of the equipment described herein.

P/N 82–7070
Revision Preliminary
January 1993

Safety Precautions

The following safety precautions should be observed while operating this instrument. Failure to comply with these precautions violates safety standards of design, manufacture and intended use of this product. Analogic Corporation assumes no liability for the customer's failure to comply with these requirements.

USE PROPER GROUNDING

A three-conductor power cord is supplied with this instrument. To minimize the hazard of shock, the instrument chassis and cabinet should be connected to electrical ground. The power cable should be either plugged into an approved, three-wire, grounded electrical outlet or used with a three-to-two-wire adapter with the ground (green) wire solidly connected to a good electrical ground at the power outlet.

HIGH VOLTAGES

Hazardous high voltages are present inside the cabinet of this instrument. Making contact with any such voltage levels could cause injury or even death. Servicing should be performed only by qualified personnel.

OBSERVE ANY SPECIAL SYMBOLS MARKED ON THE EQUIPMENT

Refer to the Instruction Manual: The instrument is marked with this symbol when the user is required to refer to the manual for special operating instructions that may prevent any hazard or damage to the instrument.

OBSERVE ALL WARNINGS, CAUTIONS AND NOTES

The operating instructions in this user's manual include special notes, cautions and warnings pertaining to the use of this instrument. Be sure to pay special attention to the following items:

WARNING: Describes a condition or action that is considered hazardous to the user, such as working around high voltages that can cause serious injury.

CAUTION: Describes a condition or action that may damage the instrument, such as applying input voltages that exceed the limitations of the instrument.

NOTE: Describes other essential information that should be brought to the user's attention, such as operating features that would otherwise be overlooked.

Warranty

Analogic warrants only to the original purchaser that this product, as purchased from Analogic or an Analogic distributor or dealer, will conform to the written specifications for a period of one year from the date of purchase. If the product fails to conform to these warranties, Analogic, as its sole and exclusive liability hereunder, will repair or replace the product and/or its components within a reasonable period of time if the product is returned to Analogic's facility at Peabody, MA, within the warranty period as expressed above. These warranties are made upon the express condition that:

a. The purchaser promptly notify Analogic in writing of any non-conformity with the above warranty including a detailed explanation of the alleged deficiencies.
b. The product is returned to Analogic at the buyer's expense only after obtaining the proper authorization from Analogic.
c. When the product is returned for repair, a copy of the original bill of sale or invoice is sent with the product .
d. Analogic will not be liable for any incidental or consequential damages.
e. In the opinion of Analogic upon inspection, the product has not been misused, altered, or damaged due to abnormal handling and/or operation.
f. Repairs to the product and/or its components have not been made by anyone other than Analogic or one of its authorized repair agents.
g. The product has not been modified, altered, or changed in any manner by anyone other than Analogic or one of its authorized repair agents.

THIS WARRANTY EXCLUDES ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, ORAL OR WRITTEN, INCLUDING WITHOUT LIMITATION WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR PURPOSE.

No term, condition, understanding or agreement purporting to modify the terms of this warranty shall have any legal effect unless made in writing and signed by an authorized officer of Analogic and the purchaser.

Contents

4 Troubleshooting and Testing

5 Semi-Automatic Calibration

6 Subassembly Replacement Procedures

List of Tables

List of Illustrations

Section 1
Introduction

1.1 SCOPE OF MANUAL

This manual provides maintenance information for the Model 2030 Multifunction Waveform Synthesizer. In general, maintaining this instrument includes periodic calibration. If a failure occurs and repair becomes necessary, it can usually be accomplished quickly by replacing the faulty field-replaceable subassembly. This manual does not cover circuit board level troubleshooting.

The information in this document is organized into the following sections:

Section 1 *Introduction*
Provides an overview of the manual and the product. Directions for getting technical assistance are also included.

Section 2 *Specifications*
Contains detailed product specifications.

Section 3 *Theory of Operation*
Describes the hardware and software operation of the instrument using functional block diagrams.

Section 4 *Troubleshooting & Testing*
Contains quick functional checks and fault-isolation procedures for tracing a failure to a field-replaceable subassembly.

Section 5 *Semi-Automatic Calibration*
Describes a semi-automatic calibration procedure using a PC running a special calibration software program.

Section 6 *Parts Replacement Procedures*
Provides instructions for removing and replacing field-replaceable subassemblies.

Section 7 *Schematic Diagrams*
Contains circuit schematic diagrams of field-replaceable circuit boards and modules.

1.2 PRODUCT OVERVIEW

The modular design of this Multifunction Waveform Synthesizer is shown in Figure 1-1. This Figure also illustrates the physical architecture of the overall system.

The front panel has a bright easy to read Liquid Crystal Display (LCD). Display contrast and brightness are adjustable by software control. The combination of display and keypad provides the user interface to the many functions of the instrument.

The CPU Board and I/O interfaces provide overall control of this system. This computer subsystem is responsible for transmitting and receiving data on the RS232 or IEEE-488 communication links, managing the front panel keyboard and display subsystems, and storing all the waveform calculation algorithms used by the Digital Signal Processor (DSP). The CPU decides which algorithms the DSP will execute and what parameters it will use in its calculations and communicates this information to the DSP on an 8-bit interprocessor bus. This CPU Board receives power from the Digital Power Supply via the DSP Board. The CPU Board also supplies high voltage to the front panel display subsystem.

The DSP Board acts as a motherboard for the CPU Board, the Digital Power Supply and the Analog Subsystem. The DSP Board lies flat on the bottom of the chassis and the CPU Board, Digital Power Supply and Analog Board stand vertically in their respective edge connectors. The DSP calculates the waveform data points and loads them into a waveform memory. The memory allows the DSP to store freshly calculated waveform data points while it simultaneously sends waveform points to the Analog Subsystem.

The Analog Subsystem consists of the Analog Board, the Filter Board and the Analog Power Supply. This subsystem is electrically isolated from the rest of the system. The Analog Subsystem receives the digital data from the DSP and creates an analog waveform. The analog reconstruction includes a high-speed digital-to-analog converter (DAC), lowpass filters, attenuators and a highly-accurate low-noise output amplifier. The main signal output floats with respect to the DSP and CPU boards, and is sent to the front and rear panels. The Analog Power Supply also floats with respect to the rest of the system.

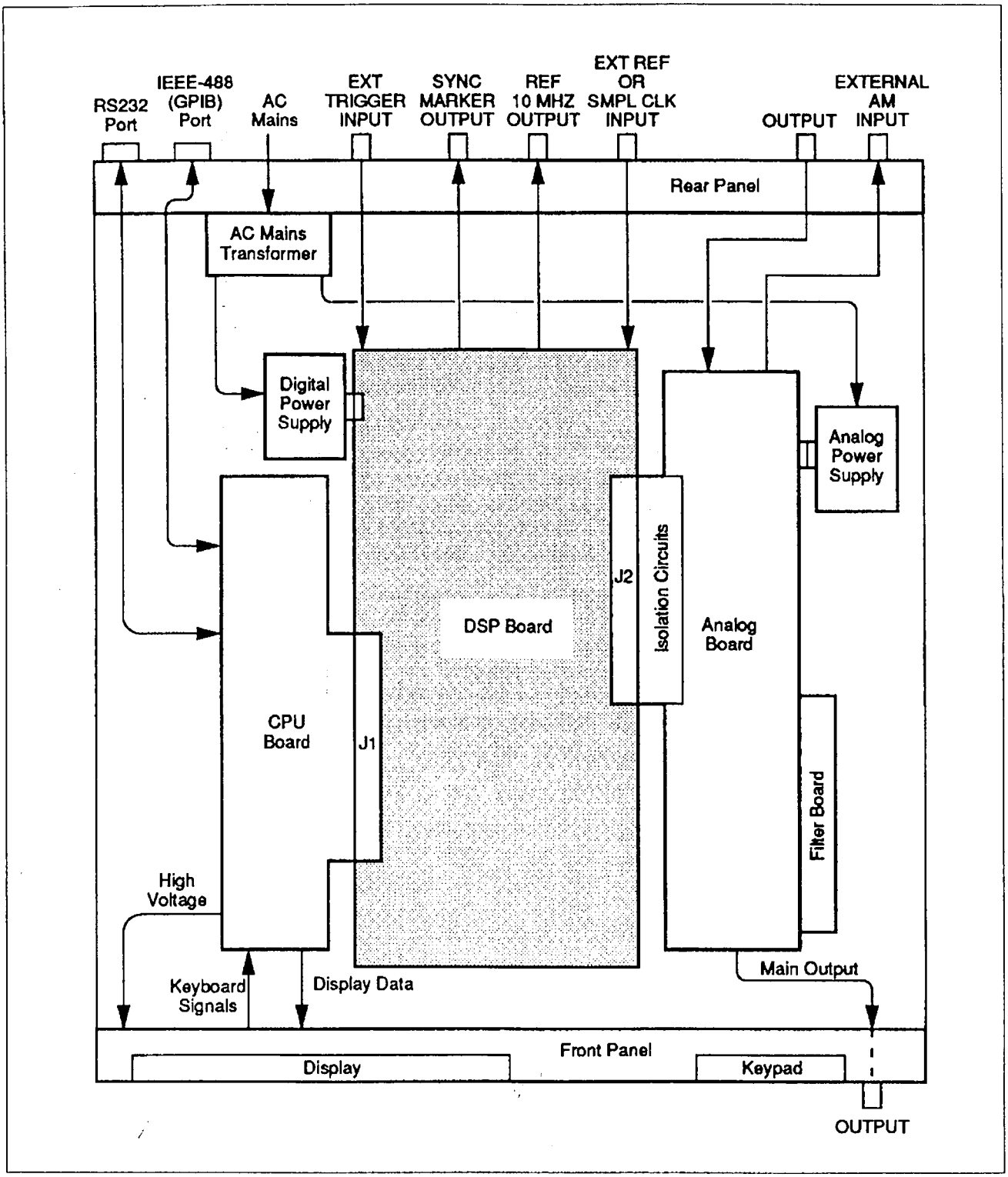


Figure 1-1. System Architecture Block Diagram

1.3 TECHNICAL ASSISTANCE

If this product fails to operate upon arrival, contact your Analogic dealer or the Measurement and Control Division (MCD) at the Analogic factory in Peabody, MA 01960 to arrange for an exchange. Upon contacting MCD Order Entry, you will be given a Return Material Authorization (RMA) number.

To arrange for an exchange, contact MCD Order Entry:

Tel: (508) 977-3000, Ext. 3871

FAX: (508) 532-6097

For technical assistance, contact MCD Applications Engineers:

Tel: (508) 977-3000
Domestic calls: Ext. 3876, 3840 or 3844
International calls: Ext. 3011 or 3844

FAX: (508) 531-1266

To arrange for service, contact the Customer Service Office:

Tel: (508) 977-3000
Repairs: Ext. 3612
Parts: Ext. 3614

Before contacting the Customer Service Office, have the following ready:

- ❑ Model number
- ❑ Serial number
- ❑ Purchase order number
- ❑ Quantity being returned
- ❑ A detailed description of the malfunction
- ❑ Your "Bill To" and "Ship To" addresses

Upon contacting the Customer Service Office, the Service Coordinator will provide you with the following:

- ❑ Customer service order number (CSO)
- ❑ Warranty status of the units being returned
- ❑ Repair charge, if any

The CSO number is your authorization number. Please write this number on your purchase order and shipping label.

Send all authorized returns to:
Analogic Corporation
8 Centennial Drive
Peabody, MA 01960
Attn: Receiving Dock B.
CSO# _____

After the material has been returned, you will receive an acknowledgement copy of the CSO which will be marked with the scheduled return date.

Section 2
Specifications

Functions

Standard Waveforms	Sine, Square, Triangle, Pulse, Ramp Up, Ramp Down, DC, Noise
Modulations and Sweeps	AM Double Sideband, Double Sideband Suppressed Carrier, AM Single Sideband, Single Sideband Suppressed Carrier, FM, PM, Decay Pulse Envelope, Sin x/x Envelope, Linear Sweep, Log Sweep
Additional Waveforms	Combined Waveforms, Arbitrary and Special Waveforms

Output

Source Impedance	50Ω/600Ω ±1% or open circuit
Amplitude Range & Resolution	5 mV pk to 9.999mV pk in steps of 1μV 10mV pk to 99.99mV pk in steps of 10μV 100mV pk to 999.9mV pk in steps of 100μV 1V pk to 10.000V pk in steps of 1mV
Amplitude Accuracy	Analog output circuitry error less than ±1% of requested amplitude at 1kHz. Typical relative error 0.05%.
Offset Range & Resolution	–10.00V to +10.00V in steps of 2.5mV
Offset Accuracy	1% ± 200 μV (20 to 30°C) ± 34 μV/°C
Freq. Range & Resolution	0.001Hz to 9.999999kHz in steps of 0.001Hz 10kHz to 99.99999kHz in steps of 0.01Hz 100kHz to 999.9999kHz in steps of 0.1Hz 1MHz to 5.000000MHz in steps of 1Hz Sinewave only: 5MHz to 20MHz in steps of 1Hz
Frequency Stability	(internal reference) 2ppm, 0 to 50°C, 2ppm/year
Relative Freq. Accuracy	±0.2 ppm ratiometric frequency error referred to Internal Reference Oscillator or External Reference Input
Noise	< 0.2mV rms with 10MHz Bandwidth; < 0.75mV rms with 1000MHz Bandwidth
Jitter	< 0.005% of waveform period +100 ps (sine); < 0.05% of waveform period +100 ps (others)
Protection	Output overloads greater than ±150mA cause opening of output relay. Safe voltage is greater than ±15V on the output connector.
Isolation	Common Mode voltages of <42V can be applied to the output connector.

Trigger

Source	Manual, External, Bus
Modes	Free Run, Counted Burst, Gated, Start, Stop, Start/Stop

Sine Wave

Frequency Range	0.001 Hz to 20 MHz
Amplitude Flatness	±0.1 dB dc to 100 kHz ±0.2 dB 100 kHz to 1 MHz ±0.3 dB 1 MHz to 20 MHz
Harmonic Distortion	–70dBc to 20kHz –65dBc to 100kHz –55dBc to 1MHz –25dBc to 20MHz
Phase Range	±360° in 0.1° increments
Phase Accuracy	±1.0° dc to 100 kHz

Triangle and Ramp

Frequency Range	0.001 Hz to 5 MHz
Nonlinearity	±0.05% @ dc to 10 kHz; ±0.5% @ 10 kHz to 1 MHz; ±2.0% @ 1 MHz to 5 MHz (10% to 90% on waveform)
Ringing	< 0.1% up to 10 kHz < 0.2% up to 5 MHz
Triangle Symmetry	User adjustable from 5% to 95% in 0.1% steps; 50nS min. risetime
Triangle Delay Range	± 1 period in steps of 0.1nS to 0.1mS, depending on frequency selected

Square and Pulse

Frequency Range	0.001Hz to 5MHz
Pulse Polarity	Positive with zero volt baseline
Duty Cycle	Adjustable from 5% to 95% in 0.1% steps (50ns minimum risetime restriction)
Delay Range	±1 waveform period in steps of 0.1 ns to 0.1 ms, depending on the frequency selected
Rise Time	15ns from .....0.001Hz to 1.47Hz 10µs from .....>1.47Hz to 1kHz 1µs from .....>1kHz to 10kHz 50 ns from .....>10kHz to 5 MHz 16 ns in Fast Square Wave (FSQR) (typ.)
Overshoot and Ringing	< 0.1% up to 10kHz; < 0.2% up to 5 MHz

Noise Function

Amplitude Range	1 mV to 1.8V rms in steps of 1 µV to 1 mV (no load)
Noise Spectral Distribution	Pseudo random with the ability to set number of spectral lines.
Amplitude Distribution	Approaches Gaussian with zero mean, depending on the selected noise record size.

Modulation and Sweeps

Modulation Types	AM DSB, DSB SC, AM SSB, SSB SC, FM, ΦM, Exponential Decay, Sinx/x
Carrier Range	1.470Hz to 20 MHz
Modulation Rate	1.470Hz to Carrier Frequency
Modulation Span	(Within 20-MHz bandwidth) AM: 0.0% to 200.0% FM: lesser of ±carrier/2 or ±2 MHz PM: ±7200 degrees
Envelope Distortion	AM: <1%
Exponential Decay Envelope	t^2e^{-at} envelope defined by peak time, duration
Sinx/x Envelope	Defined by bandwidth, repetition rate
External Modulation	0 to 40% AM
Sweeps	Linear and log

Combined Waveforms

Up to 4 standard functions can be summed or used in modulation.

Carrier	Any standard function
Modulator	Summation of up to 3 standard functions
Modulation Type	AM, FM, or PM
Postmodulation Summation	Up to 2 standard functions

Arbitrary Waveforms

Maximum Clock Rate	50MHz, 5MHz, or 384kHz internal; 25 MHz external
Waveform Length	2k to 256k points

Waveform Library

Fast Square Wave, sine cubed, sinx/x, RC lowpass/highpass filtered square wave

General

Non-volatile Memory	Over 50 instrument setups
Battery Type	Lithium BR2030
Rear Panel Inputs	Trigger, Ext. Clock/Reference, Ext. Modulation (AM)
Rear Panel Outputs	Function, 10 MHz Reference, Sync/Marker
Multi-unit Frequency Sync	Within 0.4 ppm
Interfaces	RS-232 and IEEE-488 (Model 2030A)
Operating Temperature	0 to 50°C
Power	< 30W, 100/120/220/240 Vac ±15%, 50/60 Hz Safety Class I to VDE 0411 (IEC348)
Dimensions	216 mm (8.5 in) W; 132 mm (5.2 in) H; 429 mm (16.9 in) D
Weight	6 kg (13 lb)
Mechanical Stress	Shock tested to MIL STD 810D, 40g; Vibration tested to DIN IEC 68-2--6, 5 to 55 Hz (sine) 4g rms, 80 to 300 Hz (random)

Section 3
Theory of Operation

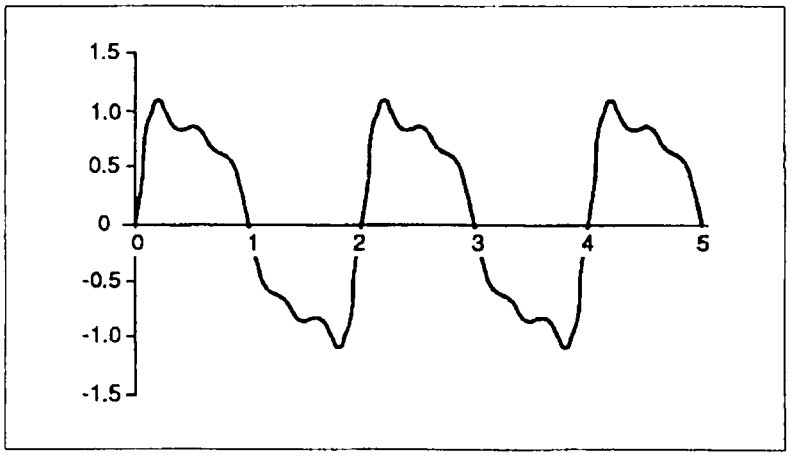
3.1 ARBITRARY WAVEFORM GENERATORS

This Multifunction Waveform Synthesizer is classified as an Arbitrary (ARB) Waveform Generator. Before describing the actual instrument that you have purchased, let's become familiar with this type of instrument.

3.1.1 Definition of an ARB Waveform Generator

An ARB Waveform Generator can produce waveforms of any shape from user-supplied information. Signal or Function Generators can only produce a small predefined set of waveform types. For example, the waveform that simulates middle "c" on the piano might look like the waveform in Figure 3-1. This function is not available on any function generator, but you can define the waveform to an ARB generator and produce the signal.

Figure 3-1. Middle C Waveform Example



Other ARB waveforms can be medical waveforms such as EKG and EEG, acoustical signals, speech simulation, sonar or radar pulses, telephone and computer modem signals, or simulated ac mains signals with added glitches and noise.

A typical ARB generator can do some or all of the following functions:

- ❑ Accept waveform data files via a computer interface (IEEE-488)
- ❑ Automatically generate standard waveforms (sine, triangle, etc.)
- ❑ Modify standard shapes by adding noise, offset, symmetry, etc.
- ❑ Automatically generate complex waveforms such as AM, FM, Sweeps, etc.
- ❑ Mathematically manipulate or combine multiple waveforms
- ❑ Entry of waveform definitions using algebraic equations

3.1.2 Typical ARB Generator Operation

Figure 3-2 shows the basic blocks of a typical ARB Waveform Generator. Waveform data, previously stored in memory, is sent to a Digital-to-Analog Converter (DAC). The data consists of a series of numbers, each of which is one point in time on the voltage waveform.

Figure 3-2. ARB Generator Basic Block Diagram

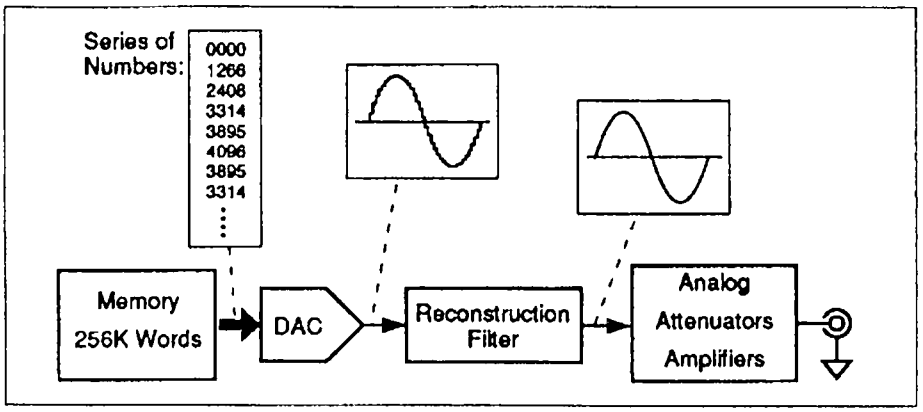


Figure 3-3 shows how the memory is structured in this application. The memory address is generated by an address counter. Its clock rate, and start and loop-back addresses are determined by the operating program of the system.

Figure 3-3. Waveform Memory Structure

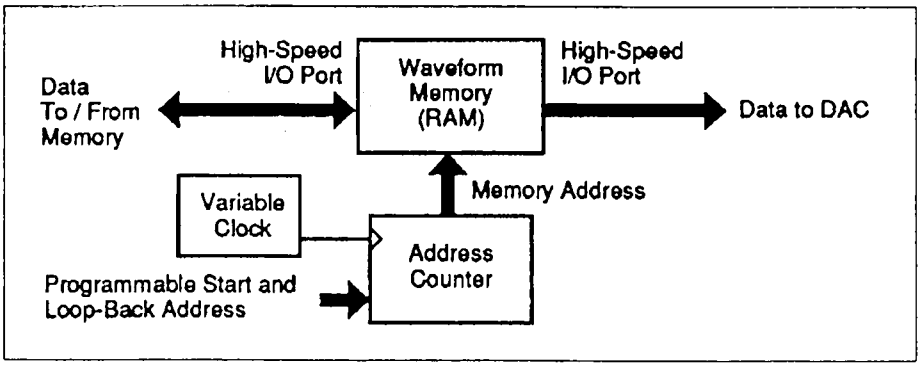
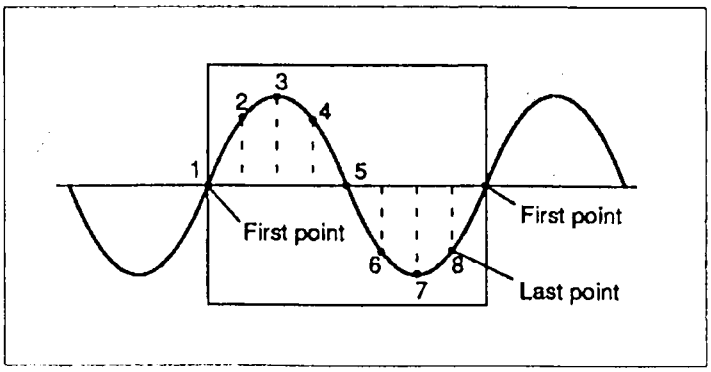


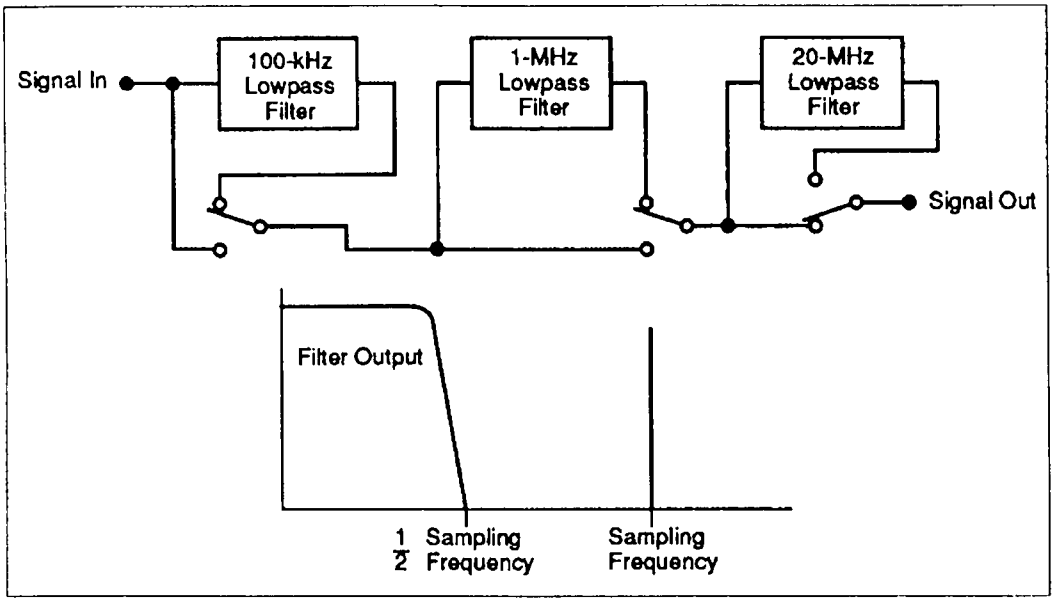
Figure 3-4 shows one cycle of a waveform based on eight points. Note that the waveform data is generated so that the last point in memory smoothly connects with the first point. The DAC receives these time samples, or numbers and generates a sampled version of the original waveform.

Figure 3-4. Waveform Data Example – 8 points/cycle



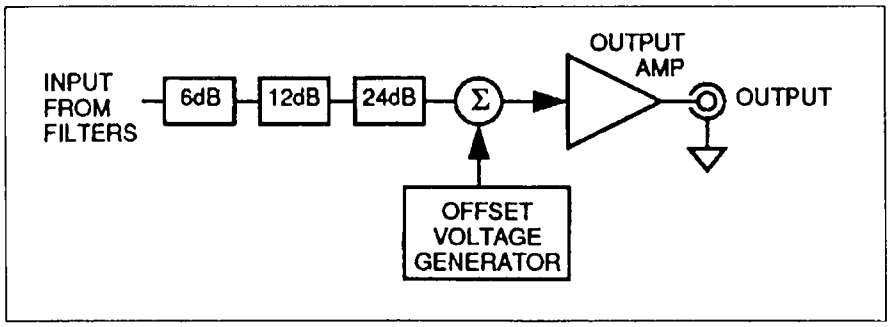
A programmable lowpass reconstruction filter (Figure 3-5) recreates the original waveform by removing unwanted signal components. This filter is usually a series of filters covering different frequency bands. The Filter must block all frequencies above 1/2 of the waveform sampling frequency.

Figure 3-5. Reconstruction Filter Block Diagram



Finally, the waveform passes through signal conditioning circuitry (Figure 3-6) before reaching the output connector. This circuitry usually includes a series of attenuators, an offset voltage circuit and an output amplifier.

Figure 3-6. Signal Conditioning Block Diagram



3.2 SYSTEM OVERVIEW

The basic functional blocks of this instrument are shown in Figure 3-7.

The CPU Board controls the overall operation of the instrument. It contains a microprocessor (μP) chip which is referred to as the Control μP to distinguish it from the Digital Signal Processor (DSP) on the DSP Board. The μP can communicate with external devices using the RS232 interface and the IEEE-488 General Purpose Instrument Bus (GPIB).

The Front Panel includes a LCD display screen, a numerical keypad interface, several software control keys ("Softkeys") and a Rotary Encoder knob. The display screen and Front Panel keys enable you to operate the instrument through the interactive Graphics User Interface (GUI).

When the CPU μP is instructed to generate a waveform, it sends commands to the Digital Signal Processor (DSP) on the DSP Board. The DSP is a very fast and powerful microprocessor. It is solely responsible for performing all the waveform point-by-point calculations and producing the waveform output of the instrument, The calculated waveform data is temporarily stored in video RAM (VRAM) before being sent to the Analog Subsystem.

Digital waveform data is sent from the DSP Board to the Analog Board in the Analog Subsystem. The Analog Subsystem is electrically isolated from the rest of the system. It is powered by a separate dc power supply and all data and control signals are transferred via magnetic couplings. The Digital-to-Analog Converter (DAC) on the Analog Board converts the pre-calculated waveform data to an analog output. The DAC output passes through reconstruction filters on the Filter Board before going to the output connectors.

This system is powered by two identical switching-regulator power supplies, one for the digital section and one for the analog section. Each is fed by separate secondary windings of a common ac line transformer. The Digital Power Supply Assembly is mounted above the DSP Board in front of the Power Input Module on the Rear Panel. The Analog Power Supply Assembly is bolted onto the Analog Board.

Figure 3-7. System Function Block Diagram

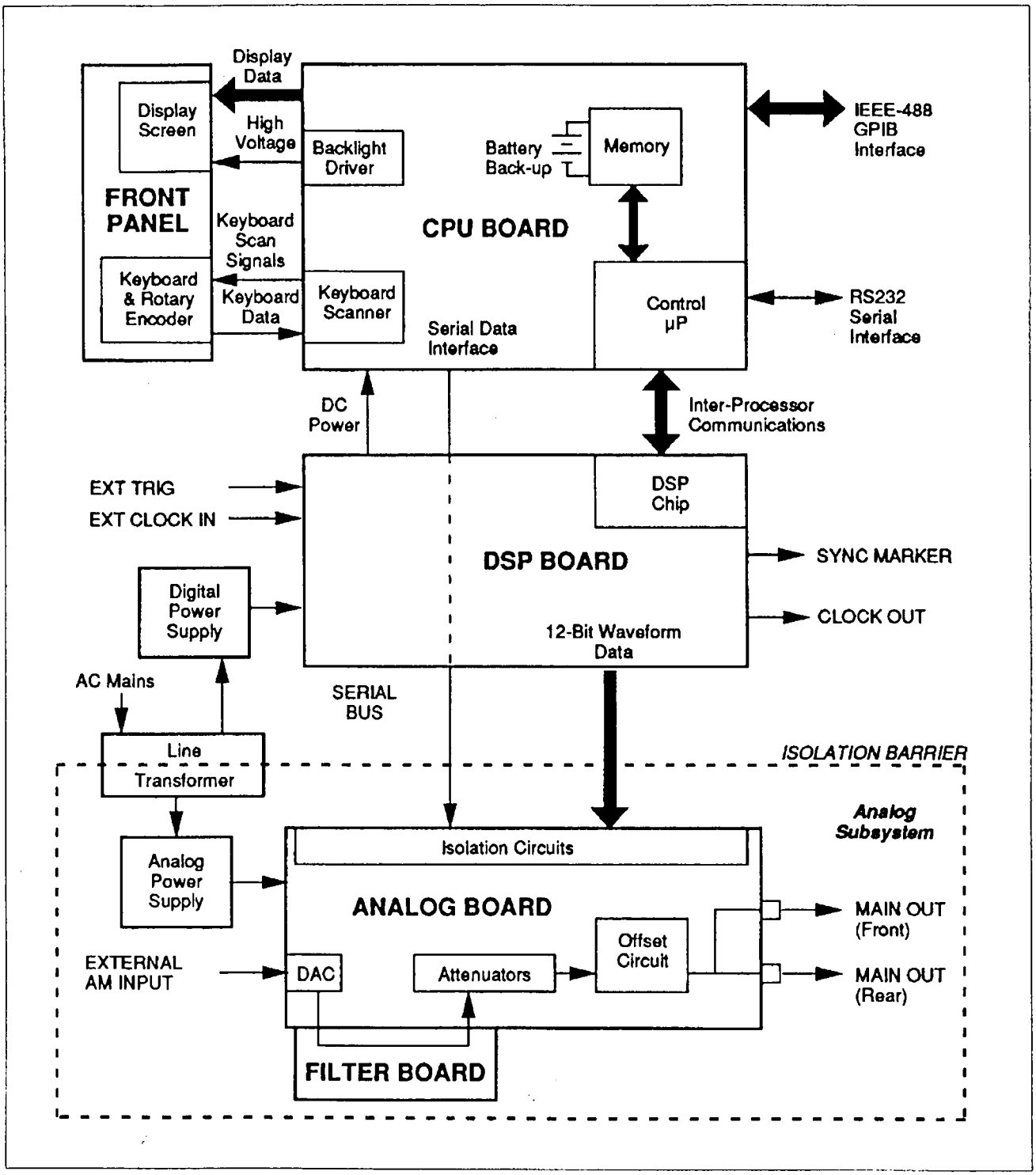
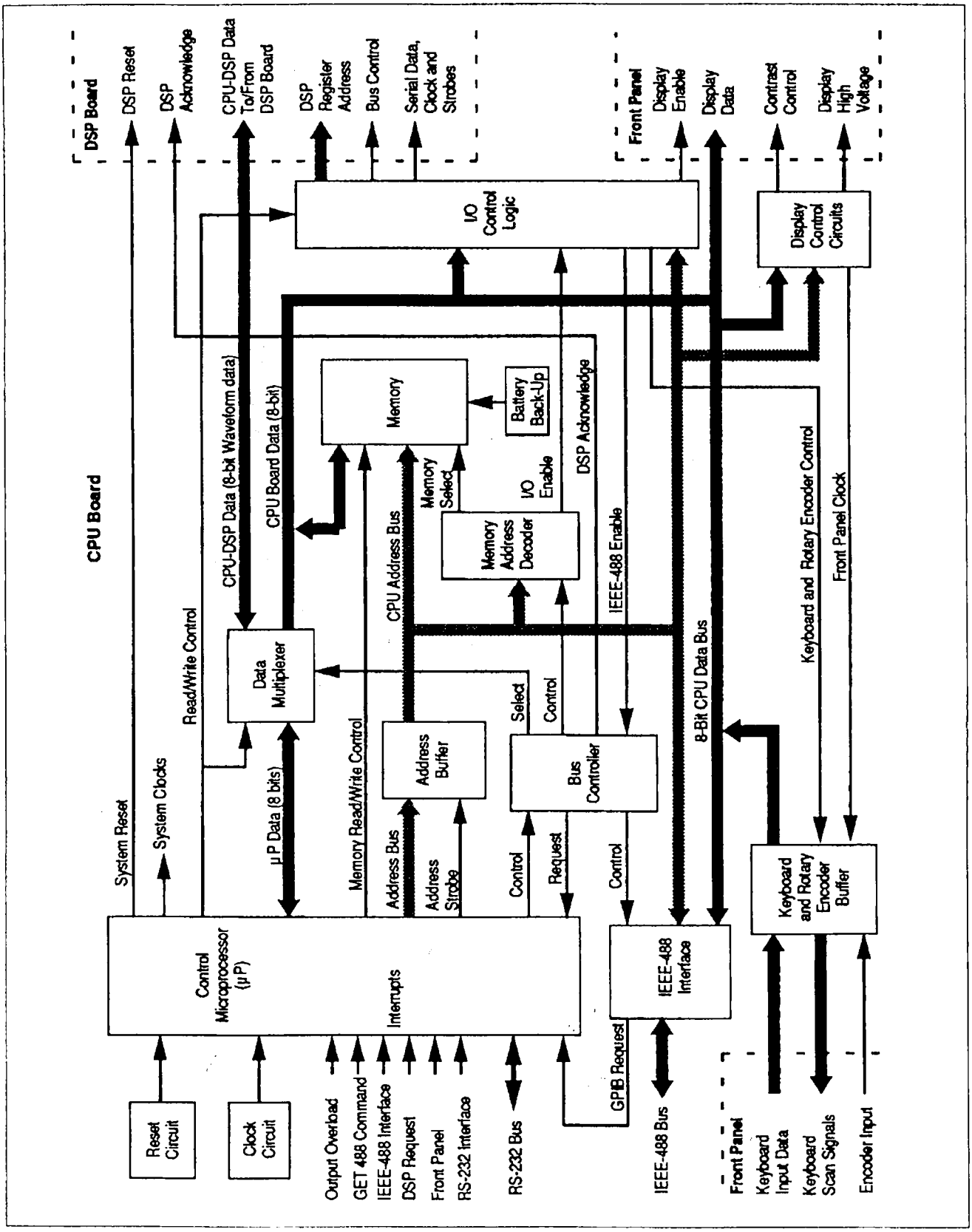


Figure 3-8. CPU Board Functional Block Diagram



3.3 CPU BOARD

The CPU Board (Figure 3-8) controls the overall operation of the instrument. It is responsible for generating the menu-driven user interface, reading the keyboard and Rotary Encoder inputs and directing the functions of the DSP. The CPU Board can communicate with external hosts or devices via the RS232 interface and the IEEE-488 General Purpose Instrumentation Bus (GPIB).

3.3.1 Control µP

The Control µP directs all functional activity of this board and the instrument based on the firmware program. The µP is reset by a Reset Circuit pulse which is triggered at power-on or whenever the reset switch is pressed on the top edge of the board.

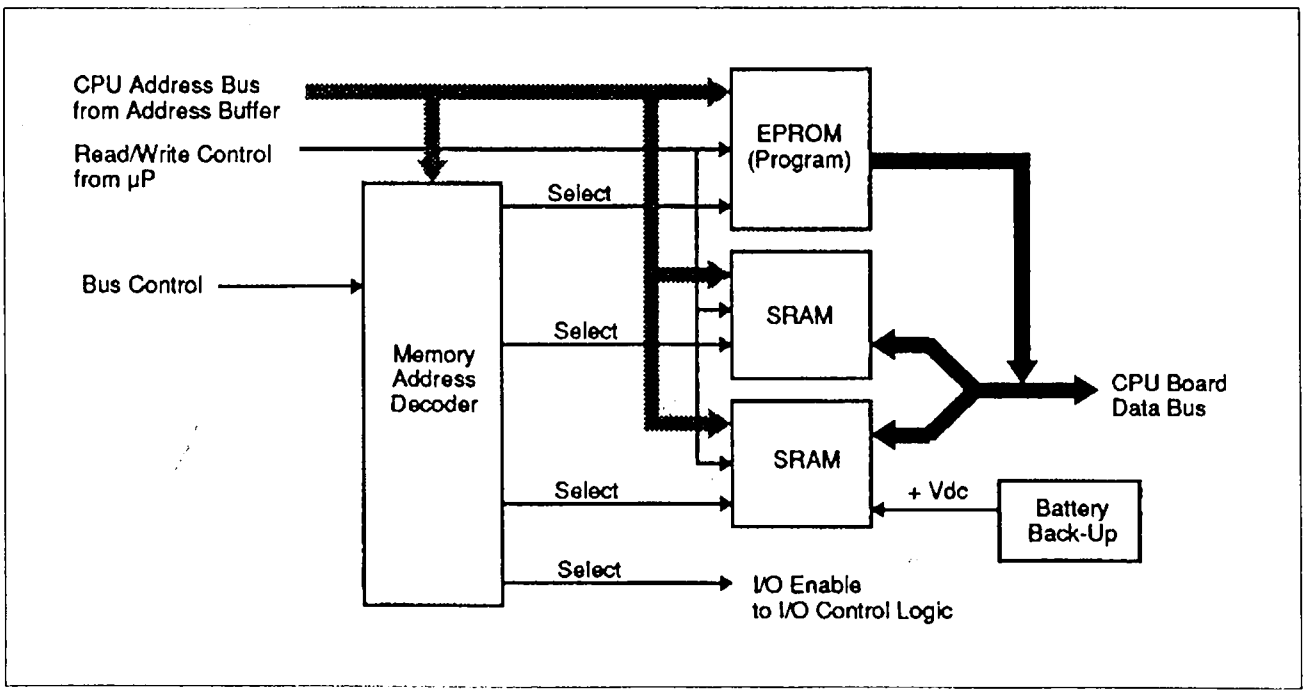
Timing for the µP and system clocks is based on a 14.7456-MHz crystal oscillator. Since the RS232 serial communications interface is included in the µP chip, the clock frequency was chosen to make the Control µP easily configurable for standard RS232 baud rates.

The µP addresses the on-board functions via the Address Buffer. Data is exchanged with the µP through the Data Multiplexer which interfaces with the DSP Board, on-board memory, the GPIB interface and the Front Panel functions.

3.3.2 On-Board Memory

On-board memory (Figure 3-9) consists of EPROM and SRAM. The Memory Address Decoder selects the appropriate memory section when the applicable memory address is on the bus. The EPROM contains the program (firmware) used to operate the instrument. Part of the SRAM is used as general data processing memory space. When the Front Panel power switch is set to OFF, a Battery Backup supply powers a small portion of SRAM which is used to store the setup of the instrument at the moment the power is removed. The Memory Address Decoder also selects the CPU-to-DSP I/O functions.

Figure 3-9. CPU Board Memory Configuration

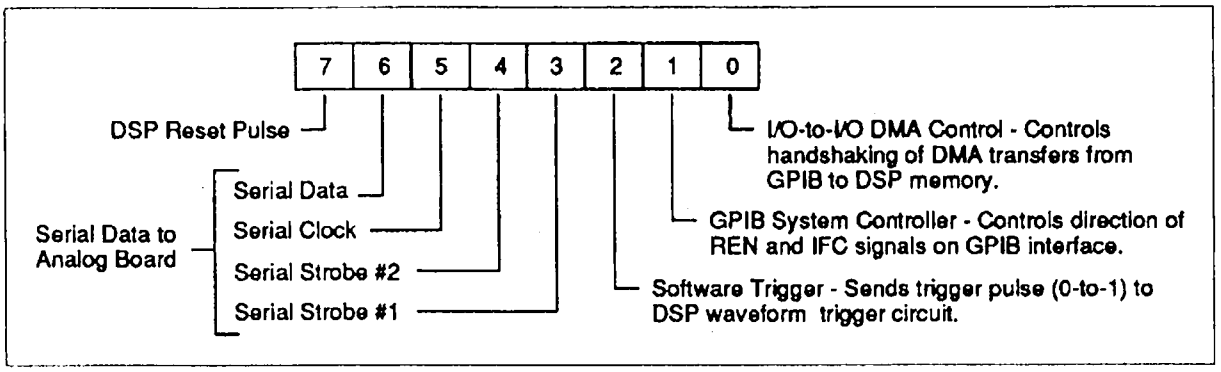


3.3.3 CPU to DSP Inter-Processor Communication

The instructions that tell the DSP Board how to calculate the waveform are sent to the DSP Board over the CPU-DSP 8-bit data bus. This information is loaded into the internal registers of the DSP chip. The DSP registers are addressed by a DSP Register Address Bus from the I/O Control Logic. The DSP Registers are described further in Section 3.4.

A general purpose register controls various DSP Board and Analog Board functions. The register format is shown in Figure 3-10.

Figure 3-10. I/O General Purpose Register Format

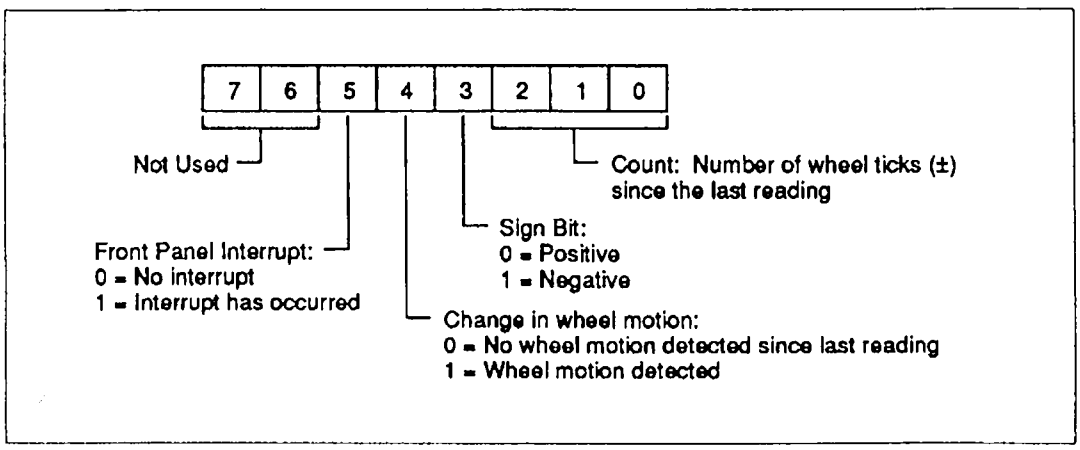


3.3.4 Front Panel Interface

The front panel interface consists of the Keyboard and Rotary Encoder Buffer and the Display Control Circuits.

A read-only Wheel Count Register (Figure 3-11) stores front panel information used by the CPU Board. When a key is pressed or the Rotary Encoder is moved, data is latched into the hardware and an interrupt is sent to the μP. This register and the Keyboard register are examined during interrupt servicing.

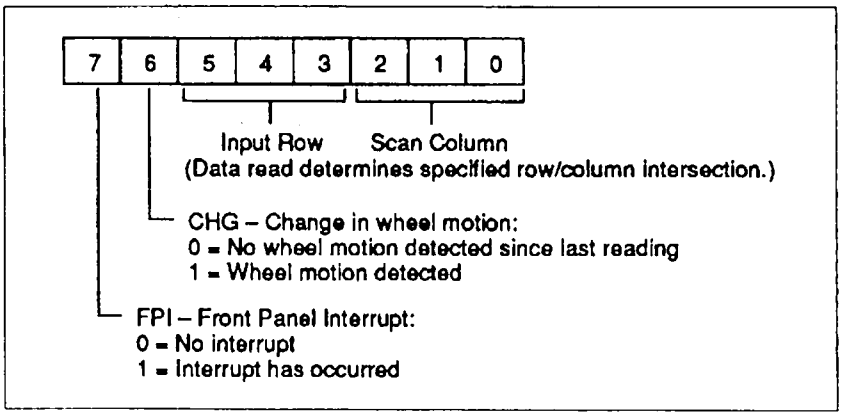
Figure 3-11. Wheel Count Register Format



The read-only Keyboard Register (Figure 3-12) works in conjunction with the Wheel Count Register described previously. Status bits FPI and CHG are duplicated so that by reading either bit the source of the interrupt is immediately determined. A Keyboard scanning signal clock is generated by a read/write counter register in a timer chip.

Display contrast is controlled by pulse-width modulation. In the timer chip, a second read/write counter register is used to control the contrast of the display screen. A third read/write counter register controls the drive signal for the display backlighting high-voltage output.

Figure 3-12. Keyboard Register Format



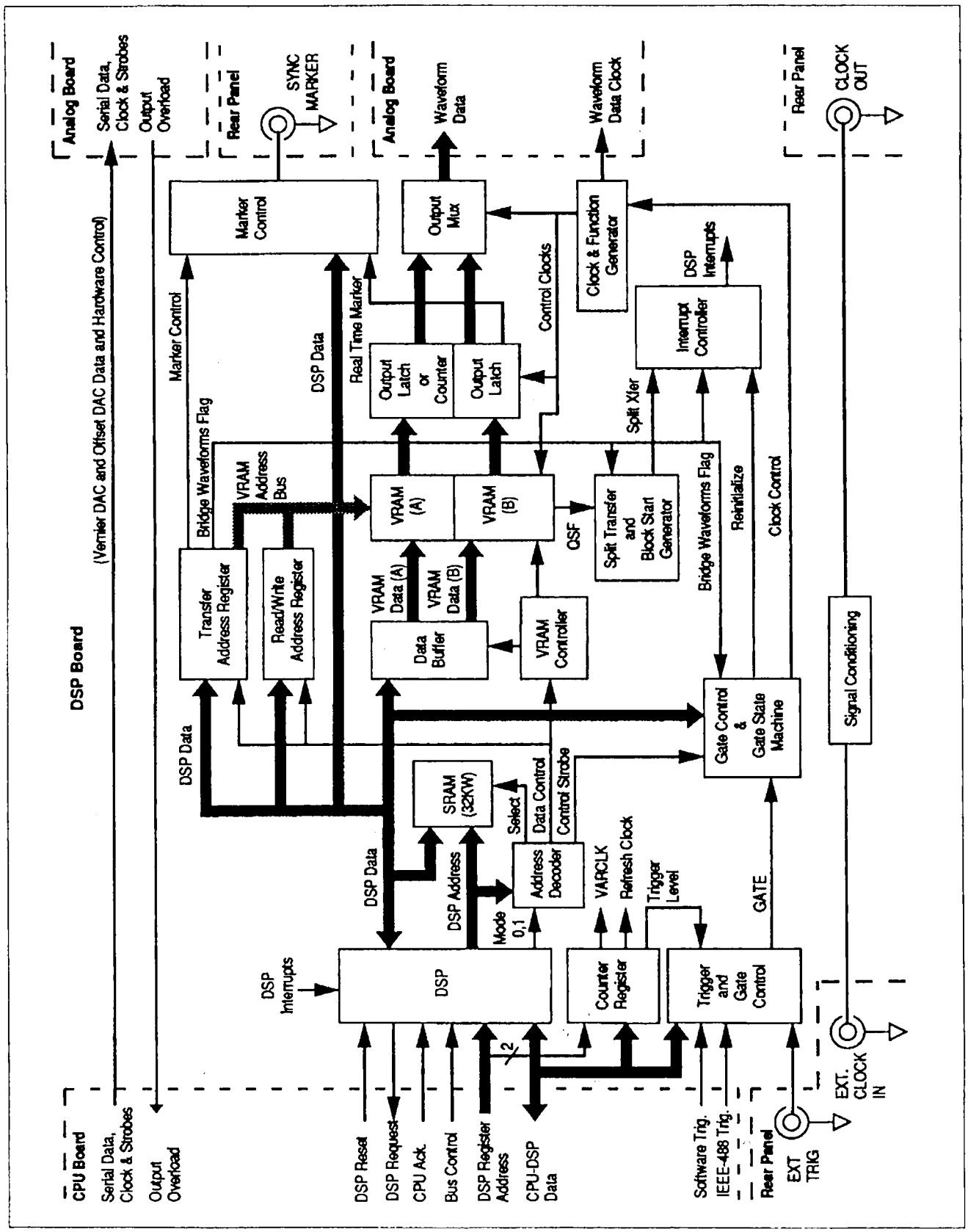
3.3.5 *Serial Interface (RS232)*

The controller for the RS232 serial communications port is located inside the µP chip. However, external line drivers are used to buffer the Transmit/Receive lines between the µP and the external connector.

3.3.6 *GPIB Interface*

The GPIB interface consists of a TMS9914 GPIB Controller chip with bus drivers to buffer signals between the chip and the external connector. This device enables the instrument to comply with IEEE-488 Standards. For more information, refer to specifications IEEE-488.1 - 1987, IEEE-488.2 - 1987, SCPI April 1990 and the TMS9914 GPIB Controller User's Guide, Texas Instruments #1602246-9701.

Figure 3-13. DSP Board Functional Block Diagram



3.4 DSP BOARD

The DSP Board (Figure 3-13) is responsible for generating a digitized waveform and transferring it to the Analog Subsystem which converts the digital data to an analog output. The DSP is controlled by instructions received from the CPU Control Microprocessor (μP).

The DSP Board basically consists of a DSP chip, 32k words of static RAM (SRAM), 512k words of video RAM (VRAM) and control circuits for various functions. The DSP Board also provides signal paths for the CPU-to-Analog Board serial interface and the Output Overload flag which are discussed in the Analog Subsystem section. The DSP Board does not affect the function of these signals.

3.4.1 The DSP Chip

The heart of the DSP Board is a low-power, user-programmable DSP chip which is a very fast and powerful processor. The CPU Boards sends instructions to the DSP to tell it how to calculate the waveform. The CPU writes these instructions into the DSP internal registers. Using the internal DSP data bus and VRAM, the DSP calculates the user-selected waveform. As the waveform is calculated, the DSP builds an address table which is used when transferring the calculated waveform to the Analog Board.

3.4.2 CPU -to-DSP Control Registers

The CPU μP controls DSP functions using internal registers in the DSP chip. The DSP Host Port Register controls CPU-to-DSP data transfers. The DSP Host Port consist of eight data bits, three address lines plus control signals. The Trigger Mode Register (Figure 3-14) is an 8-bit register that controls the trigger source and trigger type. The Counter Register (Figure 3-15) controls the variable clock source rate, trigger level and memory refresh clock rate.

Figure 3-14. Trigger Mode Register Format

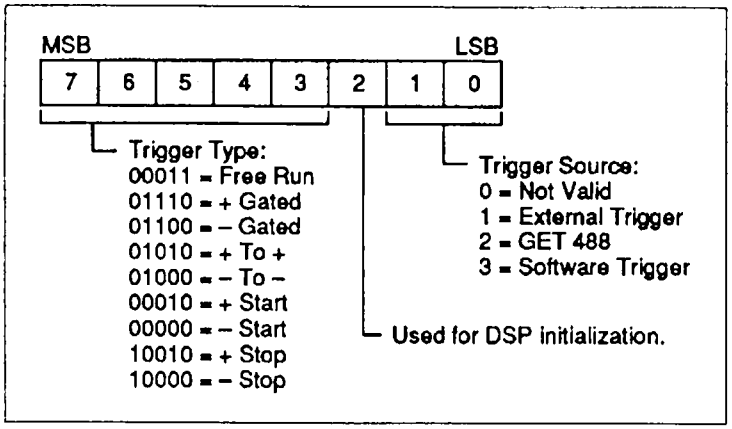
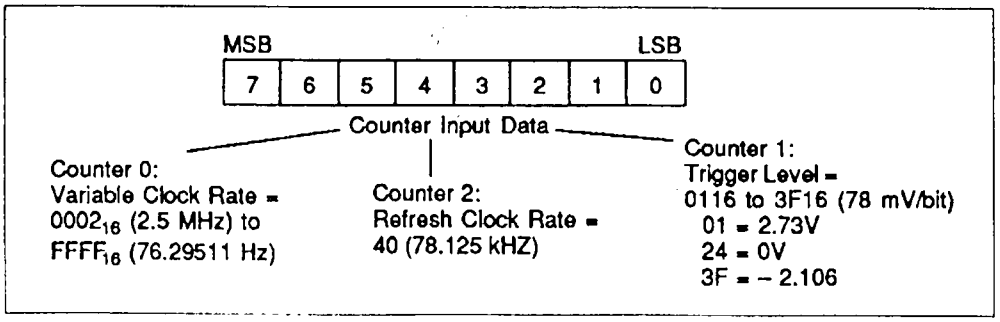


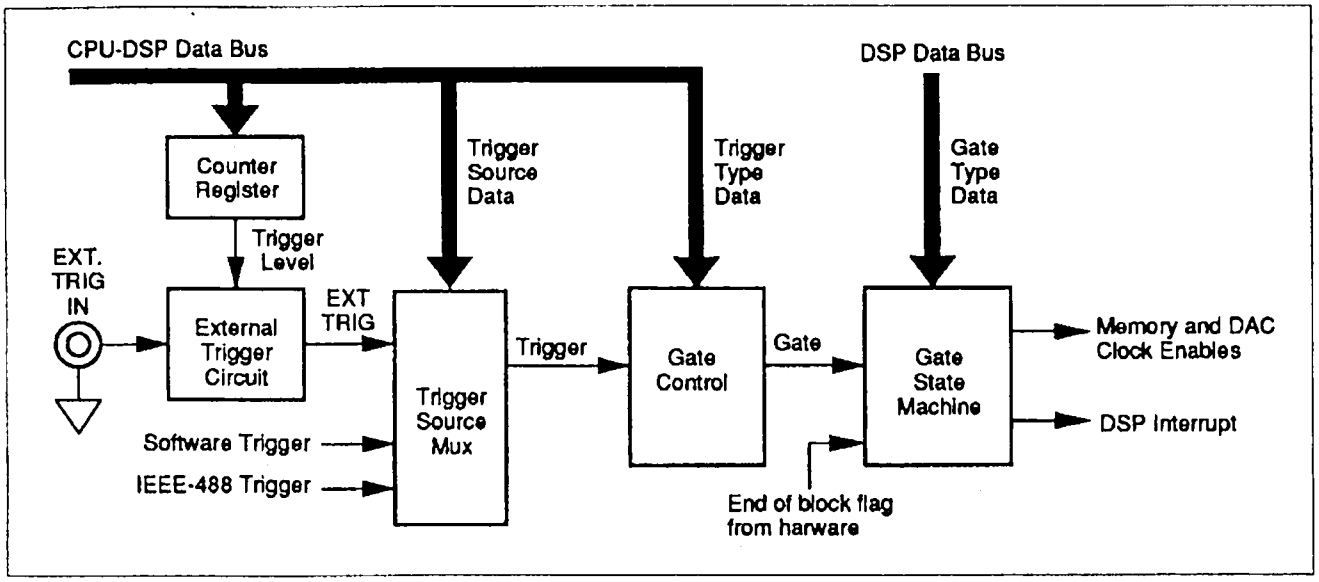
Figure 3-15. Counter Register Format



3.4.3 Trigger and Gate Control

The Trigger and Gate Control circuit (Figure 3-16) selects a trigger source from one of three inputs and produces the GATE signal. GATE is determined by the Trigger Source Data from the CPU and Trigger Type Data from the DSP.

Figure 3-16. Trigger and Gate Control Circuit



Three trigger sources are sent to the Trigger Source Mux: an external trigger, a software trigger and an IEEE-488 trigger. The multiplexer selection is controlled by Trigger Source Data from the CPU µP. The Trigger Source data is a two-bit code which selects one of three inputs. The two-bit code remains at the multiplexer input for as long as a particular trigger source is selected.

The external trigger pulse (EXT TRIG) is received from the external BNC connector on the rear panel. The External Trigger Circuit, which basically consists of a comparator chip, is similar to the trigger circuit of an oscilloscope. The Trigger Level is adjusted by an output of the Counter Register. The Software Trigger is generated by a software generated command. This can be due to a signal received from the RS232 or IEEE-488 port, or a front panel pushbutton. The IEEE-488 Trigger is a very specific type of hardware interrupt received via the IEEE-488 port ("GET" command).

The Counter Register consists of a timing chip which is programmed by the CPU Board to operate as a pulse-width modulator. The CPU µP Data changes the duration that the timing chip output is high and low. The chip output is heavily filtered to produce the dc Trigger Level signal which adjusts the trigger level of the External Trigger circuit.

The selected trigger signal is sent to the Gate Control circuit which converts trigger pulses to different types of gate signals as directed by the Trigger Type data input from the CPU µP. Trigger Type data is defined by the user-selected functions. Table 3-1 describes the Trigger and Gate output waveforms for each type of trigger.

The Gate Control and Gate State Machine are responsible for controlling the output waveform. This circuit, controlled by the Gate signal, the Gate Type Data and the Block Start flag tells the other circuits how to calculate and shape the output waveform. The Gate Type Data creates the output modes shown in Figure 3-17.

Table 3-1. Trigger Type vs. Gate Descriptions

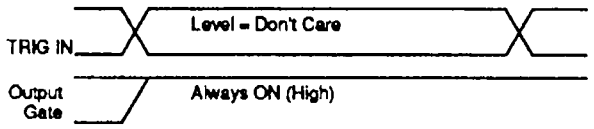
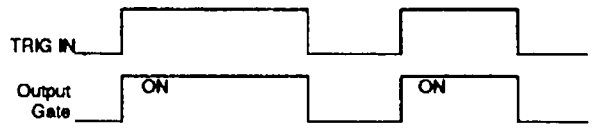
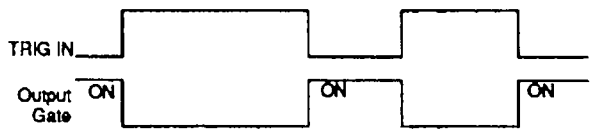
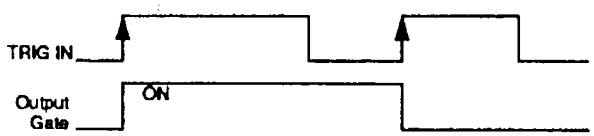
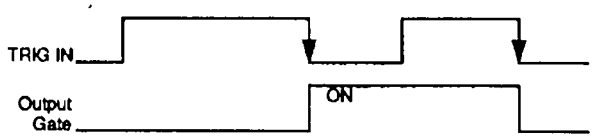
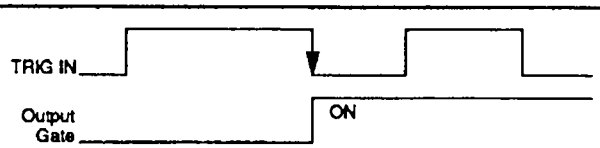
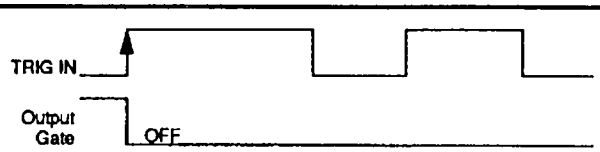
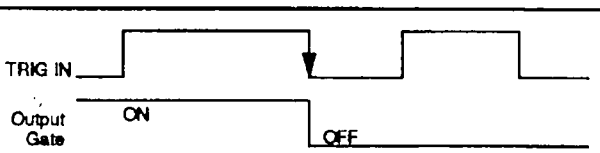
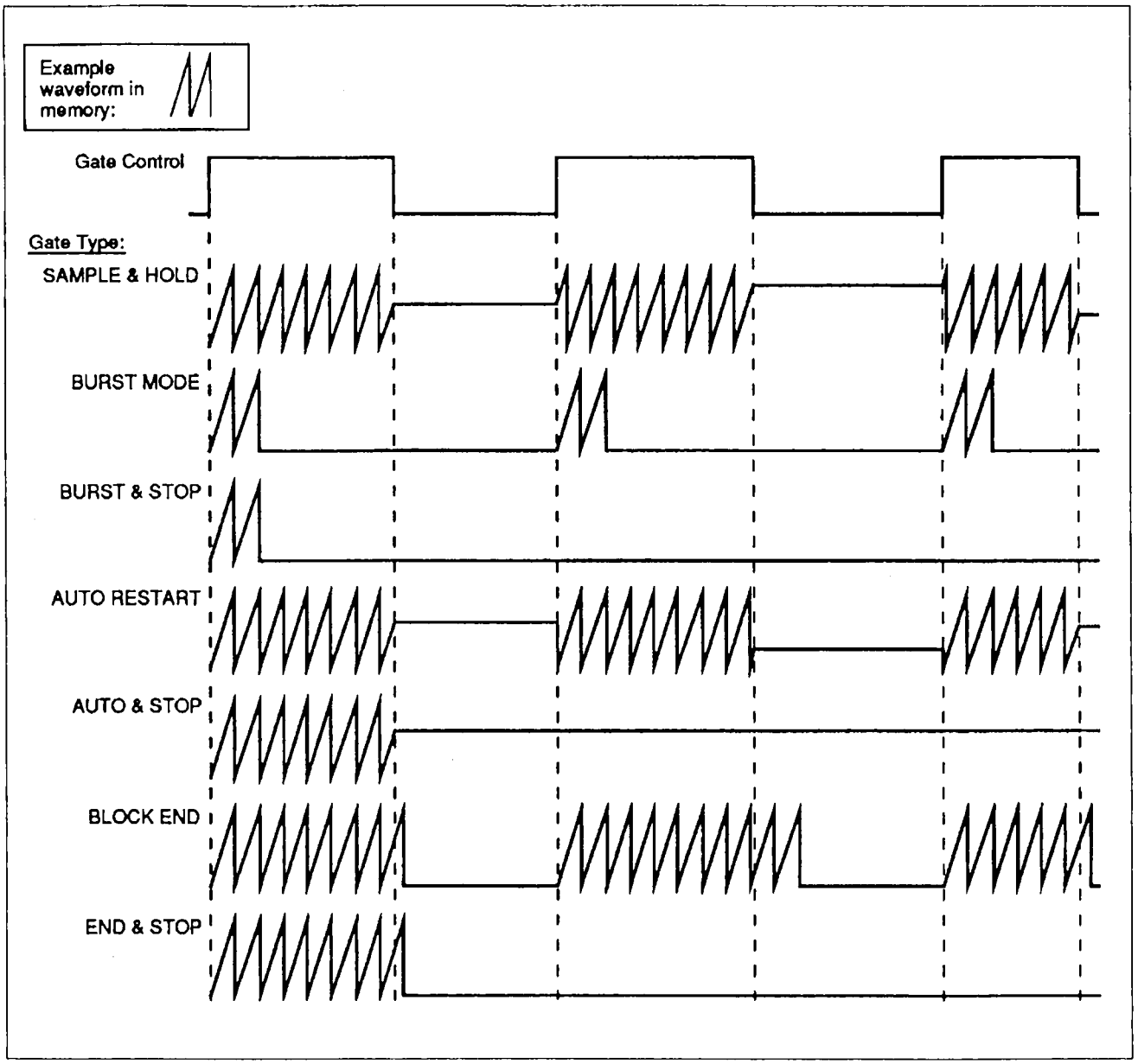
FREE RUN The simplest mode of operation. TRIG IN is ignored and the Output Gate is always ON (high) to produce an output.	
+GATED The Output Gate goes ON at every rising edge of TRIG IN and goes OFF at every falling edge of TRIG IN.	
–GATED The Output Gate goes ON at every falling edge of TRIG IN and goes OFF at every rising edge of TRIG IN.	
+ TO + On each rising edge of TRIG IN, the state of the Output Gate toggles.	
– TO – On each falling edge of TRIG IN, the state of the Output Gate toggles.	
+START On first rising edge of TRIG IN, the Output Gate goes ON and stays on, ignoring any further changes in TRIG IN.	
–START On first falling edge of TRIG IN, the Output Gate goes ON and stays on, ignoring any further changes in TRIG IN.	
+STOP On first rising edge of TRIG IN, the Output Gate goes OFF and stays off, ignoring any further changes in TRIG IN.	
–STOP On first falling edge of TRIG IN, the Output Gate goes OFF and stays off, ignoring any further changes in TRIG IN.	

Figure 3-17. Output Waveform vs. Gate

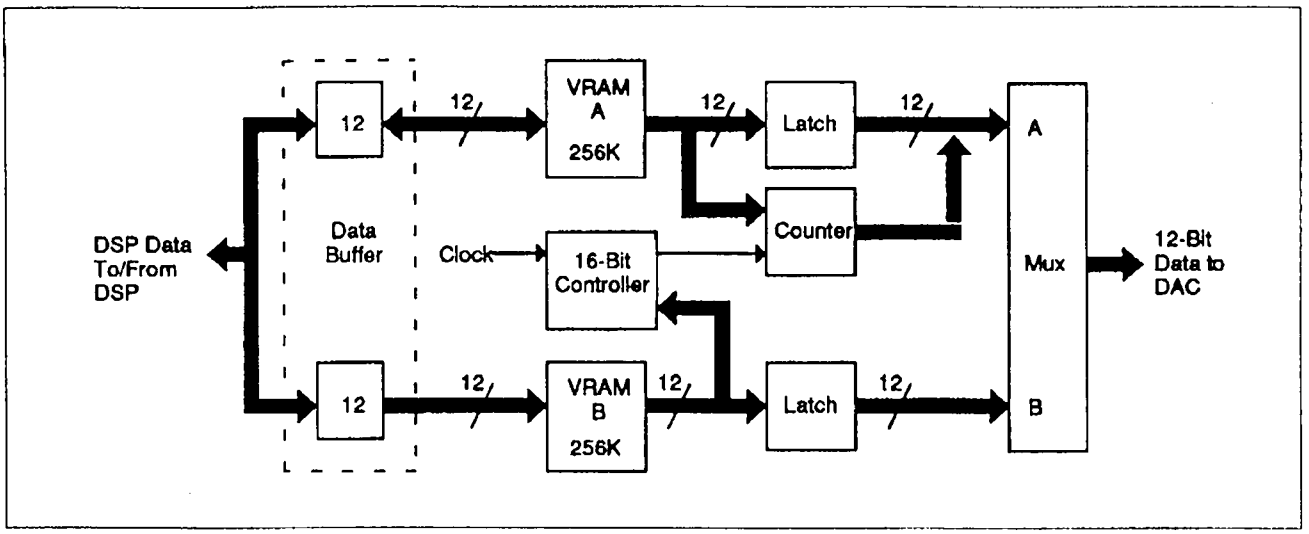


3.4.4 *Video RAM (VRAM)*

The output waveforms are sent from the Waveform Memory (VRAM) (Figure 3-18). The waveform memory basically consists of six VRAM chips configured into two banks, A and B. Each bank consists of three VRAM chips to form a 12-bit output word. Maximum speed of VRAM is 25 MHz. The memory output is held in latches before going through a high-speed, two-to-one, 12-bit output multiplexer.

Each bank of VRAM sends a 12-bit word to the A and B Multiplexer inputs. The high-speed multiplexer switches between the two 12-bit, 25-MHz inputs to create a 50-MHz input to the DAC. The switching action reads the VRAM output words in an alternating manner – one at A and then one at B, one at A and one at B again, etc.

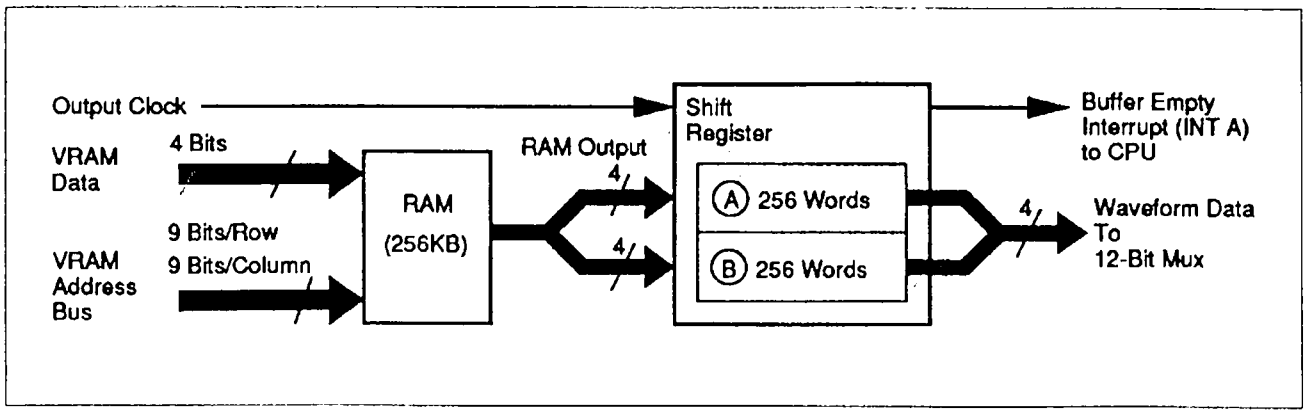
Figure 3-18. VRAM Block Diagram



The firmware normally views each 256k-word VRAM chip as two 256 k-word segments in order to perform calculations more conveniently. One 256 k-word segment of each VRAM contains the waveform currently being output while the other segment holds the next waveform to be calculated. The DSP uses these two VRAM segments in an alternating manner. When the segment currently sending out the waveform is empty, the DSP switches to the other segment to output the next waveform. While this segment is read, the first segment holds the next waveform to be calculated.

Each VRAM is a dual-port RAM using an 18-bit address (9 bits/row and 9 bits/column) and a shift register for an output stage (Figure 3-19). After receiving an 18-bit address from the transfer row and column latches, an Output Clock Pulse loads memory data into one of the two 256-word shift register buffers (A or B). One instruction can completely fill one of the shift register buffers. These two buffers, which operate independently, alternately shift out 4-bit waveform data words. While data is shifted out of one buffer, data is loaded into the other. After buffer A is empty, buffer B is read automatically – when B is empty, A is read automatically and so on. When control switches from one buffer to the other, the output stage sends an interrupt to the DSP which essentially tells the DSP that one buffer is empty and needs to be refilled while the other buffer shifts out data.

Figure 3-19. Video RAM Functional Block Diagram



At the beginning of a waveform, the VRAM is addressed and pre-calculated waveform data is loaded into buffer A. The next block of 256 words is stuffed into buffer B. The firmware then tells the system to start reading data from buffer A. When A is empty, it generates an interrupt and switches immediately to buffer B. To service the interrupt, the DSP sends another 256-word block of data to buffer A. It then goes back to what it was doing. While buffer B is shifting out data, the DSP has 256-words of time to perform other tasks before it gets interrupted again to send another block to buffer B.

The DSP returns to service the buffers every 256 output words. Meanwhile, it is busy calculating additional waveform information. For example, let's say the unit is generating a 1-kHz waveform and you change the frequency on the front panel. At that moment, the output shift register is still sending the 1-kHz waveform data. But, the DSP must now calculate new waveform data due to a change in frequency.

3.4.5 DSP Software Controls

Several registers within the DSP memory map control the waveform digitizing functions of the DSP. The VRAM Transfer Address Register is used to transfer data between two sections of memory. The digitized waveform output of the DSP Board is clocked out of the serially-accessed memory (SAM) port of the VRAM. Before data is clocked out of the SAM, it must be transferred from RAM to the SAM using this register. Data transfers can be split transfers (32 to 512 points) or full transfers (32 to 1024 points).

The VRAM Read/Write Address Register holds the address for reading or writing data between the DSP and VRAM. The Marker Data Register identifies the position of the marker within a SAM. The Control Register controls the Gate Type and a compensation function for pipeline delays in the output circuitry.

The PC Register controls the special Port C functions of the DSP chip. These functions include VRAM read/write data format, real-time interrupt enabling, memory bank switching, system clock selection and Gate State clocking.

3.5 ANALOG SUBSYSTEM

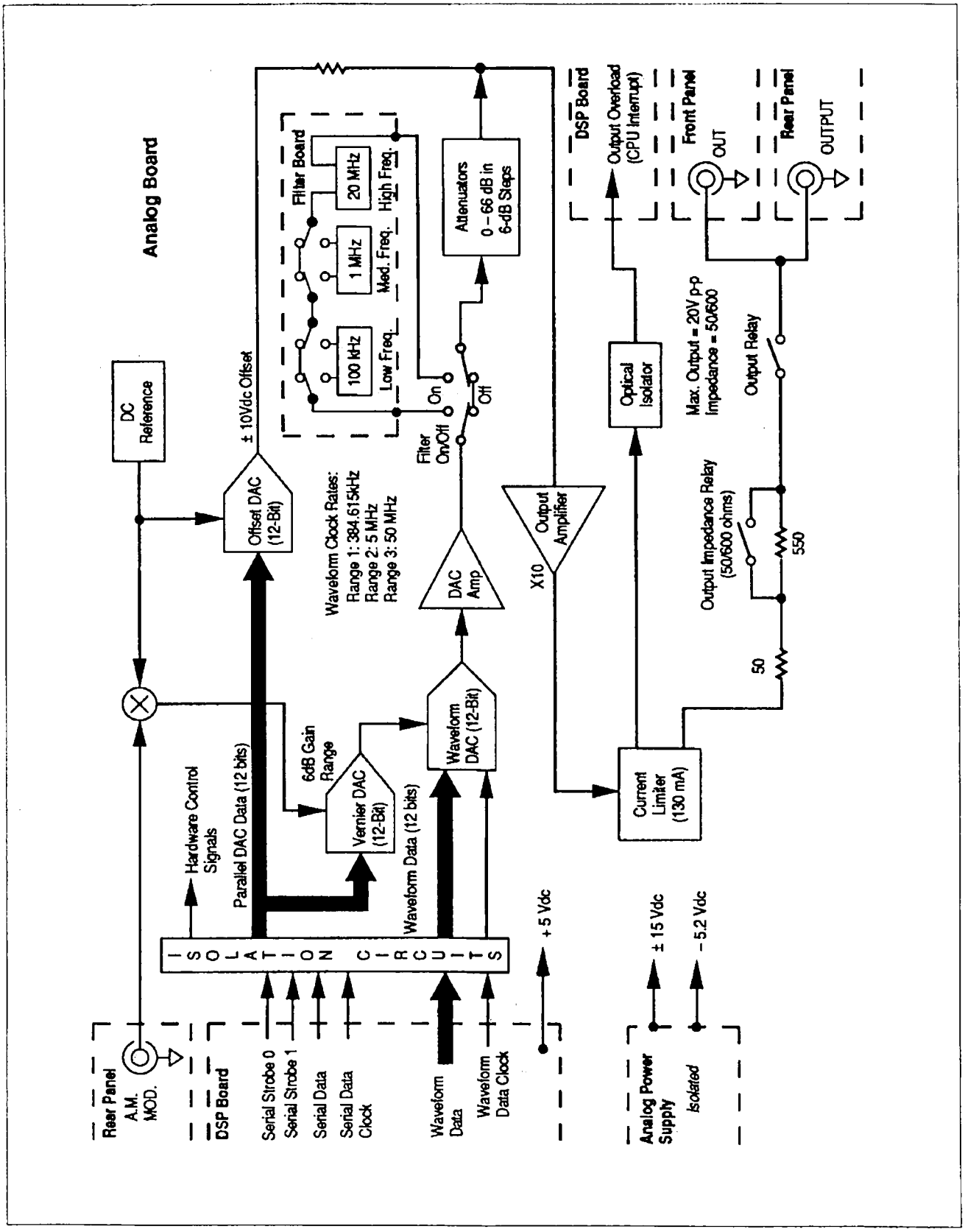
The Analog Subsystem (Figure 3-20) consists of the Analog Board, Filter Board and an isolated Power Supply. This subsystem converts the calculated digital waveform into an analog output and feeds it to the front and rear panel external BNC connectors. The Analog Board receives data and control signals from the DSP Board and external AM modulation from the rear panel BNC connector. The Analog Power Supply module is mounted on the back of the Analog Board. The Filter Board is also mounted on the Analog Board.

3.5.1 Data and Control Signal Interface

The Analog Board receives data and control signals in parallel and serial data formats from the DSP Board. The waveform data and clock are received from the DSP VRAM over a 12-bit data bus. Waveform amplitude, waveform offset data and various output controls are received serially.

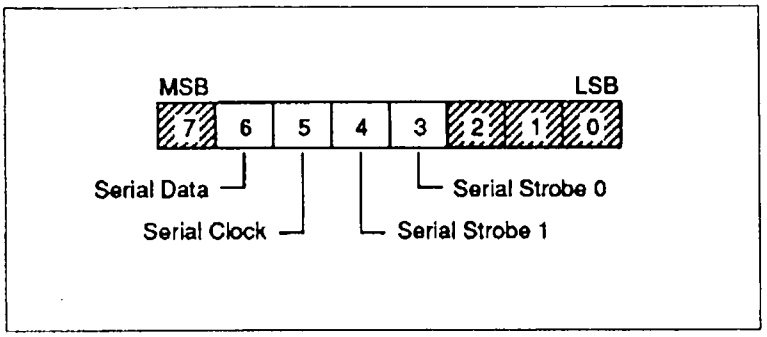
Serial and parallel data are transferred to the Analog Board through isolation circuits. Serial data is converted in the isolation circuits to 16-bit parallel data words. Twelve bits of this data are latched into the Vernier and Offset DACs by Serial Strobe 0, the remaining bits are used for control functions. Serial Strobe 1 latches data into control registers for other functions such as setting dc offset polarity, switching AM on or off, opening or closing the output relay, selecting output impedance, selecting attenuation and switching the Filter Board relays.

Figure 3-20. Analog Subsystem Block Diagram



The serial data interface is controlled by four bits in the Serial Data Interface Register (Figure 3-21). These four bits are sent from the CPU Board to the Analog Board via a path provided on the DSP Board (see Figure 3-13). The 16-bit serial data word is clocked in (MSB to LSB) by the Serial Data Clock. When all bits have been shifted in, either Serial Strobe 0 or Serial Strobe 1 latches the data into the hardware.

Figure 3-21. Serial Data Interface Register Format



Input data for the Vernier DAC and Offset DAC is latched into the hardware by Serial Strobe 0. The data format for this function is shown in Figure 3-22. Bits 12 and 13 determine which DAC receives the data word. The 12-bit Vernier DAC controls the amplitude of the Waveform DAC over a 2-to-1 range. When used with the attenuators, you can achieve fine control of the output amplitude over the full output range. The 12-bit Offset DAC controls the dc offset that is added directly to the output. The level is independent of the attenuator. However, the maximum instantaneous signal plus offset that can be tolerated on the output is ±10 volts unterminated or ±5 volts terminated.

Serial Strobe 1 latches data into the hardware to control waveform filtering, attenuation, output impedance, opening or closing the output relay, external modulation and offset polarity. The data format for this function is shown in Figure 3-23.

After power-on, the latching relays are initialized by first setting bits 5 and 8 to 14 to the opposite state and then set to the required state. Initially, the Output Relay bit (4) is automatically set to the disconnect state.

Figure 3-22. Serial Strobe 0 Data Format

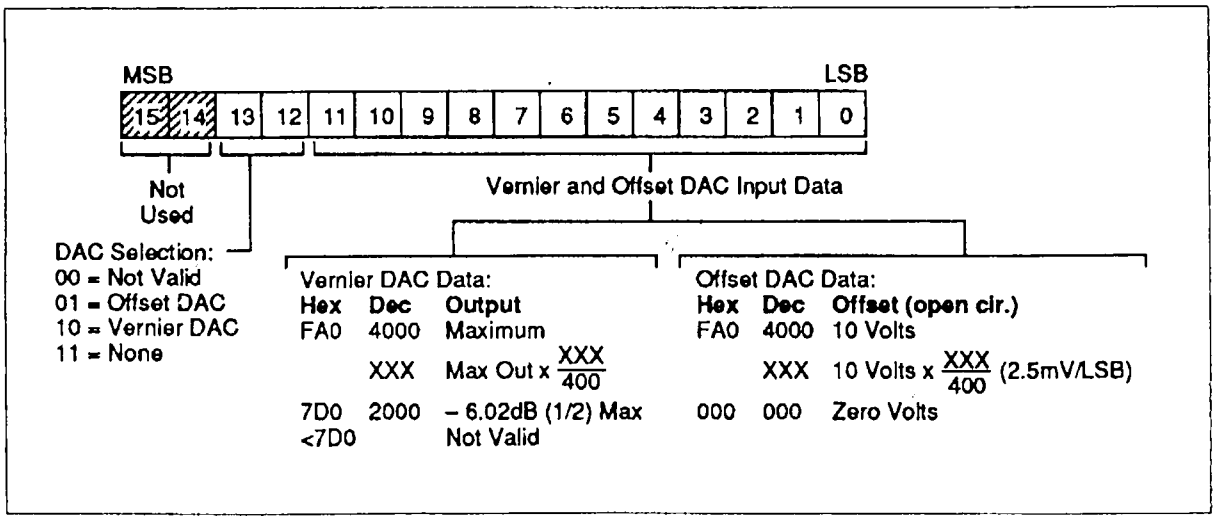
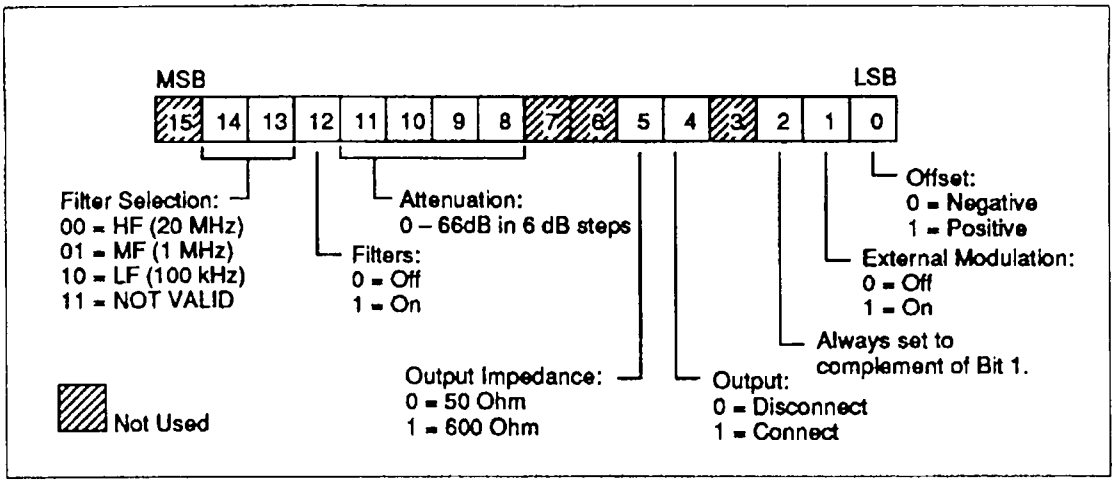


Figure 3-23. Serial Strobe 1 Data Format



3.5.2 *Digital-to-Analog Conversion*

Three 12-bit DACs are used to generate a waveform: the 50-MHz Waveform DAC, the Vernier DAC and the Offset DAC. The Vernier and Offset DACs are slow DACs compared to the 50-MHz Waveform DAC.

Parallel waveform data is clocked into the Waveform DAC to provide the main digital-to-analog conversion. This DAC is always fully loaded and always converting at its full resolution. The Waveform DAC is usually clocked at one of three rates: 390.625kHz, 5MHz or 50MHz. The frequency of the Waveform Data Clock is controlled by the DSP.

The 12-bit Waveform DAC input data word from the DSP Board generates the following range of voltages at the output of the Waveform DAC:

Data Word (Hex)	Output Level
7FF	+Maximum Output (Most Positive)
000	Zero
801	-Maximum Output
800	Minimum Output (Most Negative)

The Vernier DAC controls the amplitude of the Waveform DAC output by performing a fine adjustment of the main conversion. The Vernier DAC output is a function of the DC reference plus the AM modulation. This DAC, operating in conjunction with the Attenuators, controls the output waveform over the full output range.

The Offset DAC adds a programmed amount of dc offset (±10 volts) to the output waveform at the input to the Output Amplifier, making the dc offset level independent of the Attenuator. However, the maximum instantaneous signal plus offset that can be tolerated is ±10 volts, unterminated and ±5 volts, terminated. The offset polarity is controlled by data bit 0 in the Serial Strobe 1 data word. The Output Amplifier has a gain of 10 and provides a 10-volt peak-to-peak output into a 50-ohm load or 20 volts peak-to-peak open circuit.

3.5.3 *Waveform DAC Output Filtering*

The three filters on the Filter Board are used in conjunction with the Waveform DAC clocks to reconstruct the output waveform. These filters are program-selectable by the CPU Board via the Serial Data Interface. The controlling data bits (bits 12-14) are latched into the hardware by Serial Strobe 1.

3.5.4 Attenuators

The Attenuators are connected together in various combinations by relays to provide 0 to 66 decibels of attenuation in 6-dB steps. The relays are controlled by serial data bits 8-11 in the Serial Strobe 1 data word.

3.5.5 Current Limiting

The Current Limiter monitors the output current. If the output current exceeds 150 milliamps, the Current Limiter circuit sends the Output Overload signal to the CPU Board via a path provided on the DSP Board. Output Overload causes a CPU Board interrupt – the CPU sets a data bit in the serial data stream which is latched into a hardware register by Serial Strobe 1 and opens the Output Relay.

3.5.6 Output Impedance Selection

The output impedance of the instrument is set to 50 or 600 ohms by closing or opening the Output Impedance Relay. This is controlled by bit 5 in the Serial Strobe 1 data word.

3.5.7 Output Signal Control

The Output signal is placed on the output connector when the Output Relay is closed. This is controlled by bit 4 in the Serial Strobe 1 data word. This relay is opened when an Output Overload signal is sent to the CPU.

3.6 POWER SUPPLY MODULE

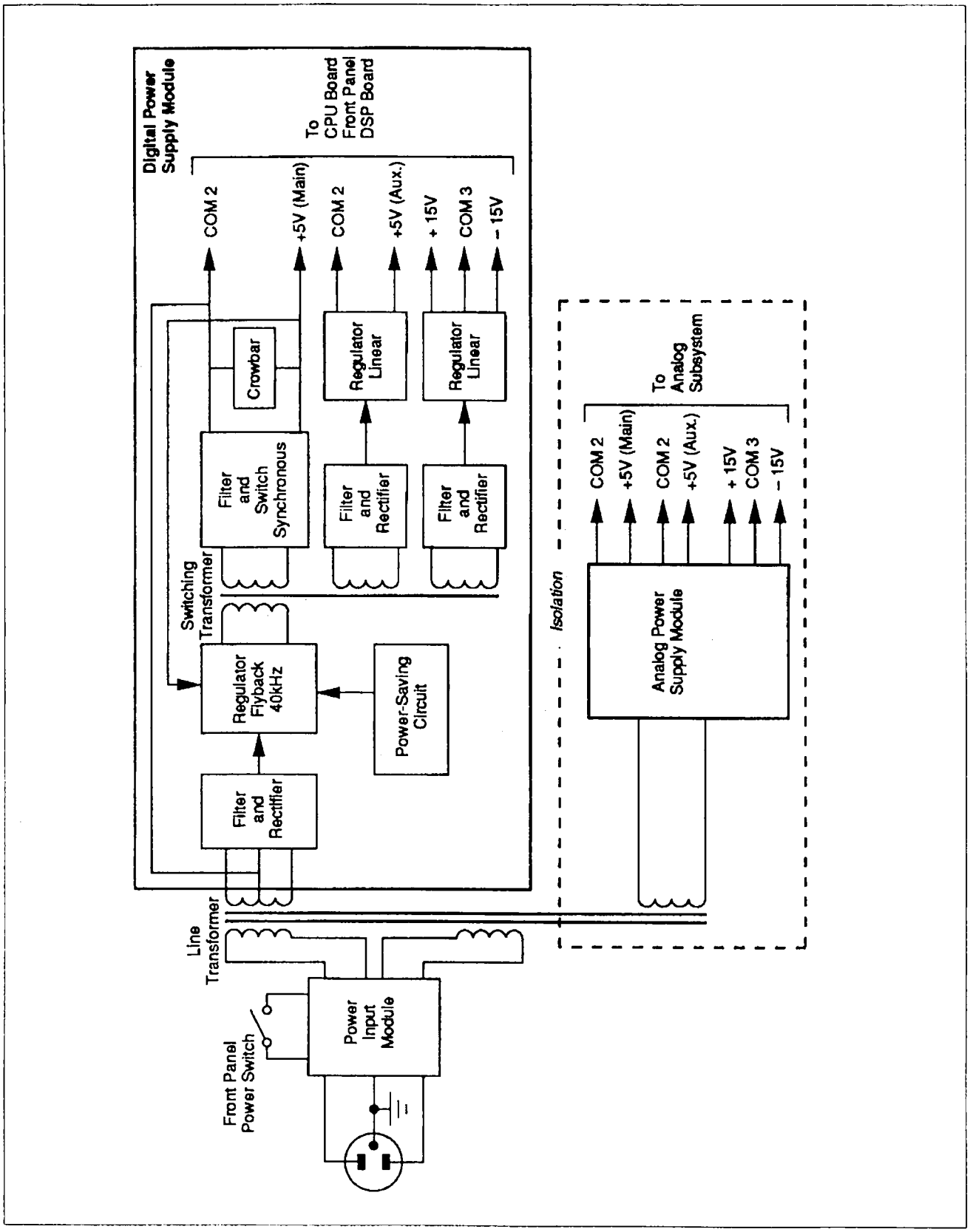
Both the Analog and Digital power supply modules (Figure 3-24) receive ac voltage from the same line transformer. The line transformer receives the ac mains input via the power entry module on the rear panel of the instrument. The power entry module contains an input filter, the line fuses and line voltage selection switches.

Each power supply module uses a flyback switching regulator and linear post regulation to produce ±15 volts and two 5-volt outputs (main and auxiliary). The ±15-volt and auxiliary 5-volt outputs are isolated from each other and from the main 5-volt output. The main 5-volt output shares a common with the primary side regulator and the center tap of the line transformer secondary.

The ac input from the center-tapped 50/60 Hz line transformer is fed into a rectifier and filter to produce a raw 23-volt supply (nominal). A 40kHz flyback regulator converts the raw 23 volts dc into 40-kHz duty cycle modulated power which is applied to the primary of a ferrite core transformer on the power supply module. The switching regulator senses the main 5-volt output and regulates the flyback duty cycle as appropriate to maintain a constant output voltage. A power-saving circuit initially supplies power to the switching regulator circuit from the raw 23-volt dc supply and switches to the 5-volt supply once the system is running.

A synchronous switch and filter convert ac from the switching transformer secondary to dc for the main 5-volt output. A crowbar circuit across the output protects the system from catastrophic over-voltage. For the auxiliary supplies, rectifier and filter circuits produce partially-regulated dc voltage from the switching transformer secondary windings. The linear post regulators then provide tightly-regulated, low-ripple 5-volt and ±15-volt outputs.

Figure 3-24. System Power Supply Functional Block Diagram



Section 4
Troubleshooting and Testing

4.1 INTRODUCTION

This section includes troubleshooting and testing information used for isolating failures to a field-replaceable subassembly. Several quick functional checks are provided which can be used to verify that the basic functions of the instrument operate as specified.

4.2 RECOMMENDED TEST EQUIPMENT

The following equipment is recommended for troubleshoooting:

- ❑ Tektronix Model 2465 High-Speed Oscilloscope or equivalent
- ❑ Tektronix 7A22 Differential Input Scope Plug-In or equivalent
- ❑ HP3458A AC-DC Voltmeter or equivalent

4.3 QUICK FUNCTIONAL CHECKS

These quick functional checks do not require removing the covers from the instrument. All checks are performed at the front and rear panels using bench test equipment. The results of these checks are only general indicators of the problem. To further isolate the problem to a subassembly, see Section 4.4.

4.3.1 Power-On Check

If you are experiencing trouble, it is important to first check that the instrument is inititalized properly at power-on.

(1) Check that the Power Input Module on the Rear Panel is set for the correct ac line voltage. If incorrect, refer to your User's Manual for instructions on changing the line voltage setting.

(2) Set Front Panel power switch to ON.

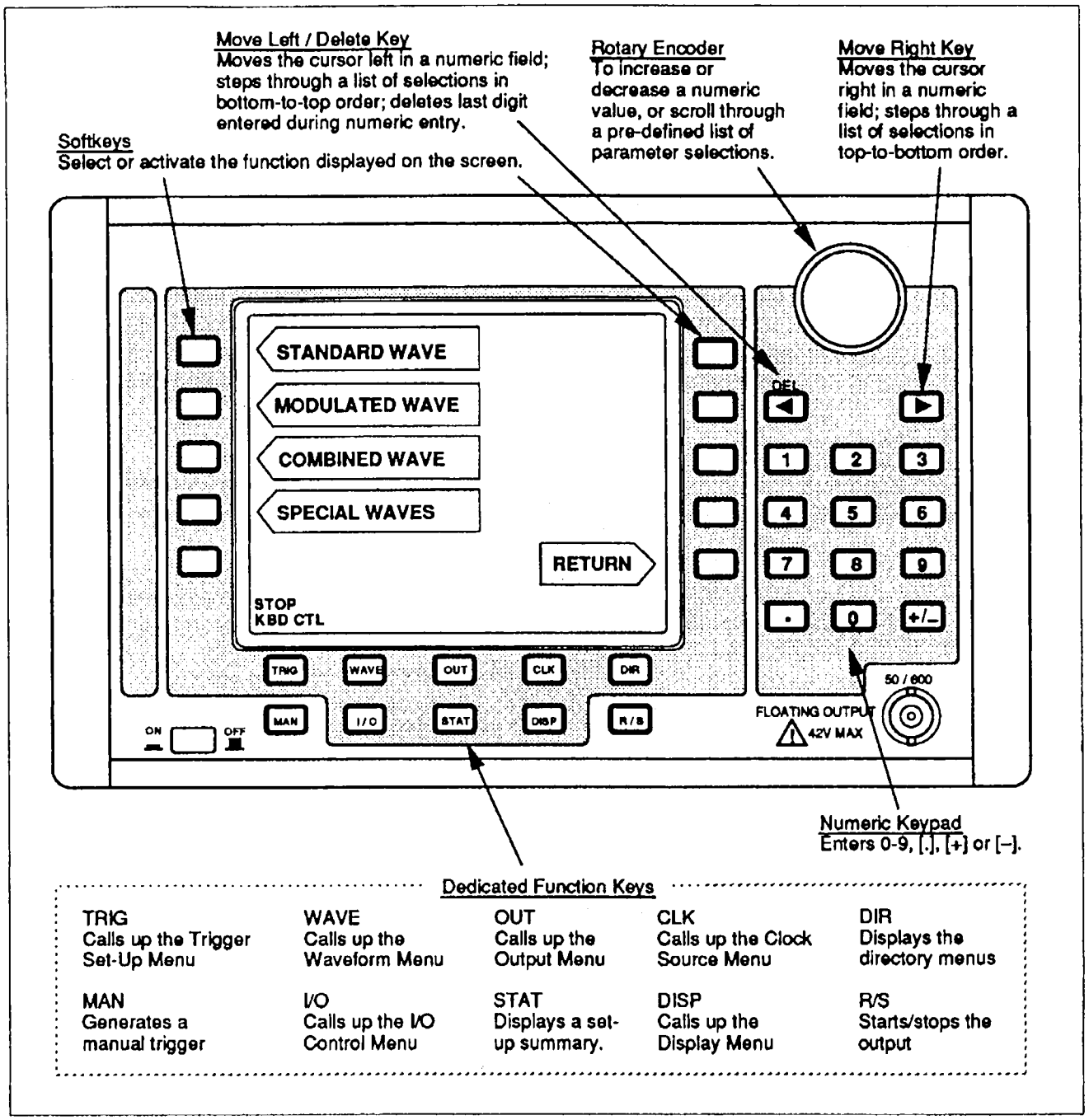
(3) Note that the instrument performs a self test during which the manufacturer's name and the firmware revision number are displayed briefly on the display screen. When the power-on process is complete, the display screen will show whatever display was on it when the power was set to OFF.

(4) If the instrument fails to follow this sequence, either the CPU Board, the Front Panel Assembly or the internal power supplies could be faulty. If necessary, see Section 4.4 for further troubleshooting. See Section 6 for parts replacement procedures.

4.3.2 Front Panel Checks

Operating the Front Panel keys tests the user Interface of the instrument. Any malfunctions discovered here may point to a faulty Front Panel Assembly or CPU Board. Referring to Figure 4-1, verify that all keys perform their respective functions. Refer to your Hardware User's Manual if you need more information about local operation.

Figure 4-1. Front Panel Key Functions



If you detect a malfunction, replace the CPU Board first to correct the problem. If the problem still exists, replace the Front Panel or Display Cable Assembly. If necessary, see Section 5 for further troubleshooting. See Section 6 for parts replacement procedures.

4.3.3 *Quick Output Checks*

(1) Using a BNC-to-BNC cable, connect the oscilloscope to the front panel main output.

(2) Run and verify any waveform. If no output, see Section 4.4.

(3) Move the cable from the Front Panel connector to the Rear Panel OUTPUT connector and verify that the output is identical. If no output, see Section 4.4.

(4) Move the cable from the Rear Panel OUTPUT connector to the REF 10MHZ OUTPUT connector. Verify signal on oscilloscope. If no output, see Section 4.4

(5) Move the cable back to the Front Panel main output connector.

(6) Run and verify each type of waveform using the oscilloscope. If any output problems are detected, see Section 4.4.

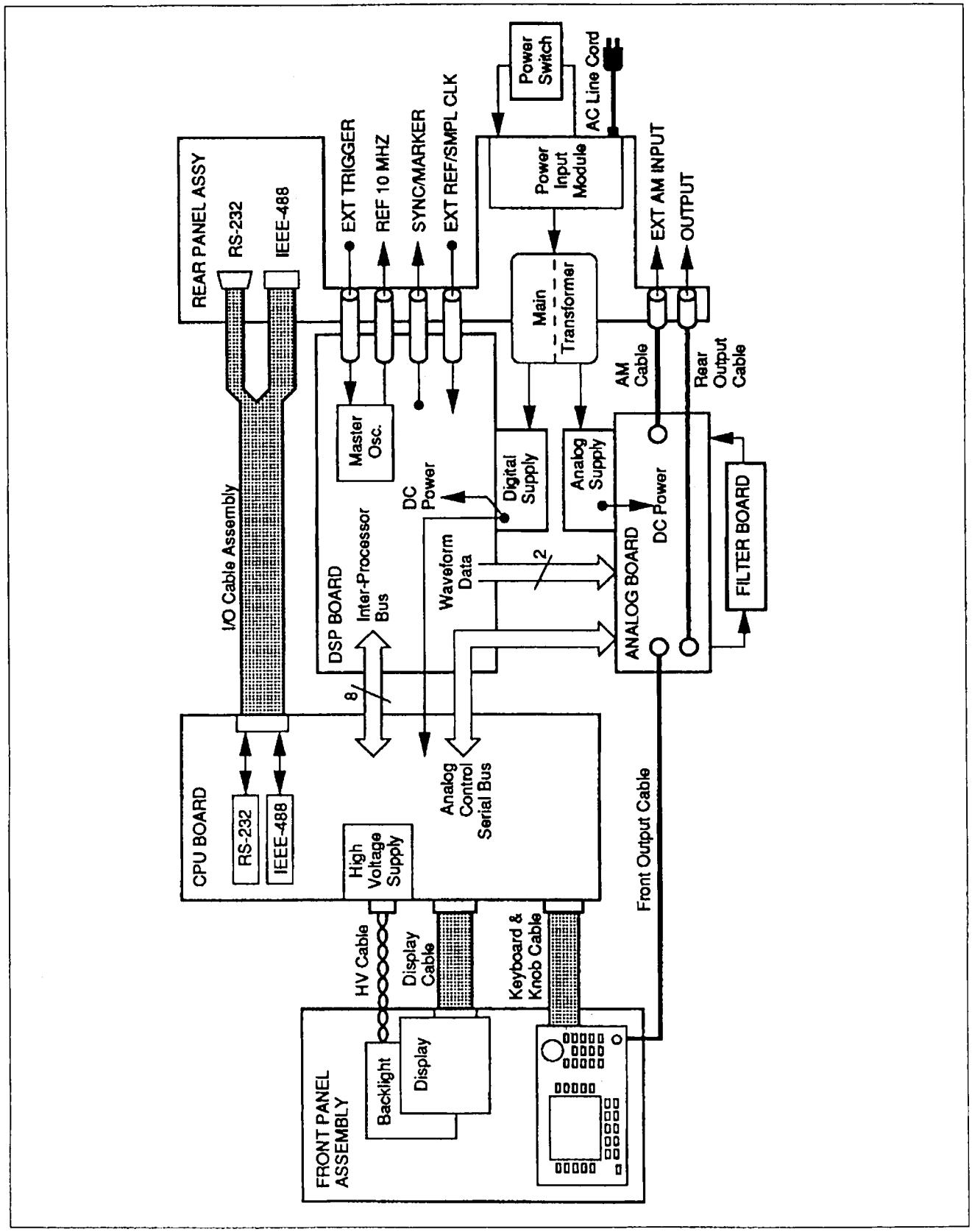
4.4 ISOLATING FAULTY SUBASSEMBLIES

Table 4-1 and Figure 4-2 are provided to help you isolate failures to a system subassembly. Figure 4-2 is a pictorial summary of functional activity within the system. Table 4-1 is a guide to locating the faulty subassembly. Locate the type of failure detected in the left-hand column of the table and follow the recommended action as listed in the right-hand column.

Table 4-1. Troubleshooting Table

Failure	Recommended Action
No Backlight.	1. Replace CPU Board. 2. Replace Digital Power Supply. 3. Replace Front Panel Assembly.
Backlight on but not adjustable.	Replace CPU Board.
Display scrambled, blank, or dead rows/columns.	1. Replace Front Panel Assembly. 2. Re-initialize CPU and NVRAM (see Section 4.5). 3. Replace CPU Board.
No front or rear output.	1. Swap front and rear output cable connections on the Analog Board (P4 and P6). Check outputs again to isolate bad cable, replace if found. 2. Replace Analog Board.
No external AM input.	1. Replace EXT AM input cable. 2. Replace Analog Board.
No RS-232 or IEEE-488 communication.	1. Replace I/O Cable Assembly 2. Replace CPU Board. 3. Replace Digital Power Supply.
Problems with: Trigger, Sync/Marker Output, Ref. 10MHz Output, Ext Ref. OR Sample Clock input; or oscillator "out of lock".	1. Run DSP diagnostic routines (see Section 4.5). 2. Re-initialize CPU and NVRAM (see Section 4.5). 3. Replace CPU Board. 4. Replace Digital Power Supply. 5. Replace DSP Board.
Wrong waveform offset, amplitude or output impedance.	1. Replace Analog Board 2. Replace CPU Board. 3. Replace Analog Power Supply.
Waveform corrupted.	1. Re-initialize CPU and NVRAM (see Section 4.5). 2. Replace CPU Board. 3. Replace Analog Power Supply. 4. Replace DSP Board.
Power-up diagnostic errors	Replace CPU Board.
User interface locks up.	Re-initialize CPU and NVRAM (see Section 4.5).

Figure 4-2. Functional Summary Block Diagram



4.5 CPU/NVRAM RE-INITIALIZE PROCEDURE

(1) Set the power swtich to OFF.

CAUTION: High voltage is generated inside this instrument. Be careful when operating the instrument with the Top Cover removed.

(2) Remove the Top Cover.

(3) Place an insulator, such as a piece of paper, under the plus terminal of the battery holder to disconnect the battery (Figure 4-3).

(4) Carefully, attach one end of a clip lead to the chassis and momentarily touch the other end of the lead to the plus terminal of the battey holder to remove any stored charge.

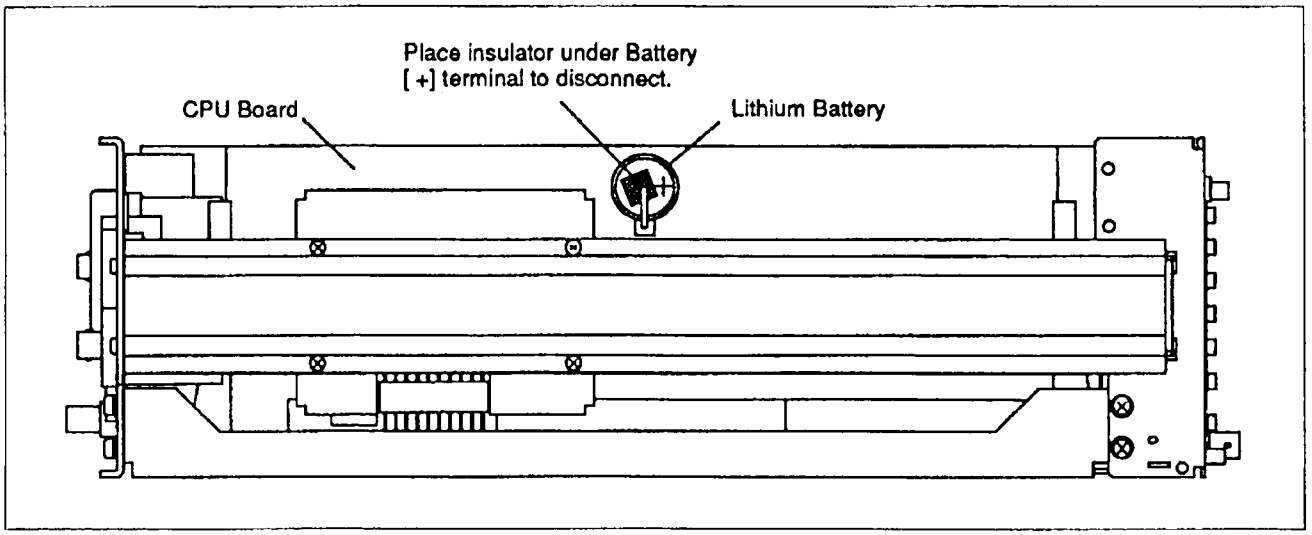
CAUTION: Do not ground the plus side of the battery itself.

(5) Remove the insulator from the battery terminal to connect the battery.

(6) Replace the Top Cover.

(7) Set the power to ON.

Figure 4-3. Disconnecting the Battery on the CPU Board



4.6 DSP DIAGNOSTIC TESTS

The firmware of the instrument contains three diagnostic tests to check the performance of the Digital Signal Processor (DSP) Board. These tests exercise the DSP chip, its internal memory, the external memory and the waveform output memory. All tests are accessed by command over the GPIB interface.

To set the instrument to the test mode, send

```
WAVE=TEST
```

To select a test, send:

```
DSP_TEST=<test number>
```

To run the test and receive the results, send:

```
DSP_TEST?
```

To return to a normal operating mode, set the instrument to one of the waveform modes:

```
WAVE=STD  . . . for Standard Waves
WAVE=MOD  . . . for Modulated Waves
WAVE=COMB . . for Combined Waves
WAVE=ARB  . . . for Arbirary Waves
```

NOTE: ***"DSP_TEST=<test number>" must be sent before each "DSP_TEST" query.***

Table 4-2. DSP Tests

No.	Name	Successful Results
2	DSP Internal Memory Test	DSP_TEST= 22
3	External Memory Test	DSP_TEST= 33
4	Waveform Output Memory Test	DSP_TEST= 44

Table 4-3. DSP Test Failure Messages

Message	Meaning
DSP_TEST= XX	Test failed.
DSP_TEST= NO TEST	Test was not specified before sending DSP_TEST?
DSP_TEST= NO UPLOAD	Failure to communicate with the DSP.

4.7 POWER SUPPLY VOLTAGE CHECKS

Replacing a power supply may be avoided by measuring the output voltages first to determine if a failure has occurred. The following procedures describe how to access test points on the Digital and Analog Power Supplies.

4.7.1 Digital Power Supply Voltage Check

The Digital Power Supply output voltages can be measured on the connector of the Digital Power Supply. To gain access to this connector and measure the voltage outputs, do the following:

(1) Set the power switch to OFF.

(2) Disconnect the ac line cord from the Power Input Module on the Rear Panel.

(3) Remove the Top Cover (Section 6.2.2) and Rear Cover Assembly (Section 6.2.3).

(4) Plug the ac line cord into the Power Input Module and set the power switch to ON.

(5) Referring to Figure 4-4, locate the Digital Power Supply connector and measure the voltages using a digital multimeter.

4.7.2 Analog Power Supply Voltage Check

The Analog Power Supply output voltages can be measured on the connector of the Analog Power Supply. To gain access to this connector and measure the voltage outputs, do the following:

(1) Set the power switch to OFF.

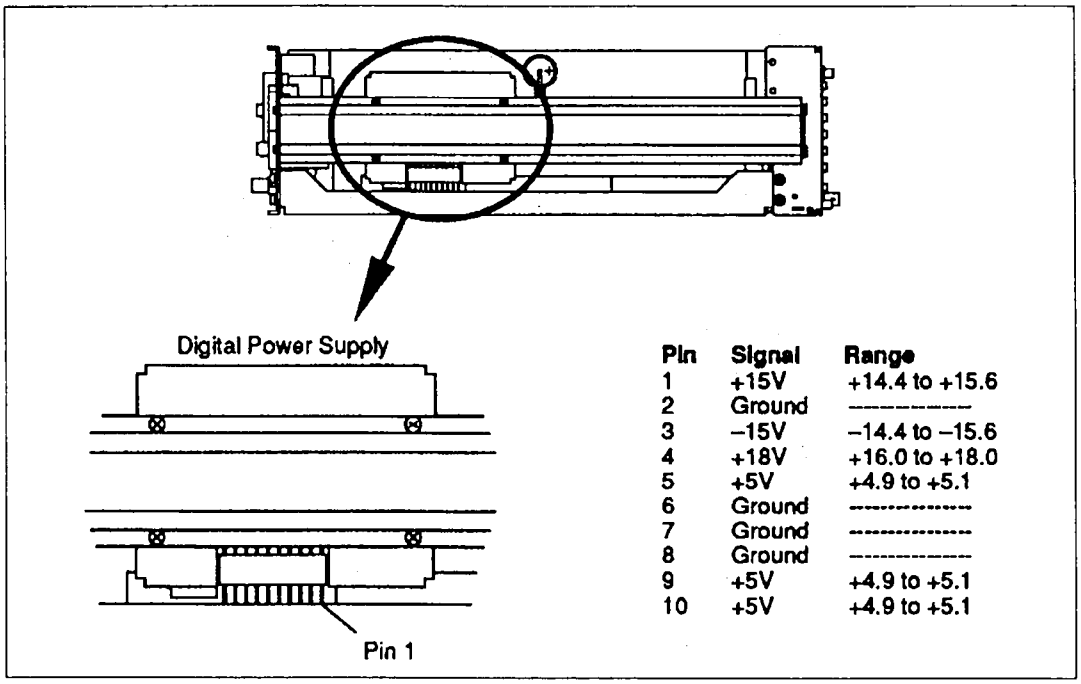
(2) Disconnect the ac line cord from the Power Input Module on the Rear Panel.

(3) Remove the Top Cover (Section 6.2.2).

(4) Plug the ac line cord into the Power Input Module and set the power switch to ON.

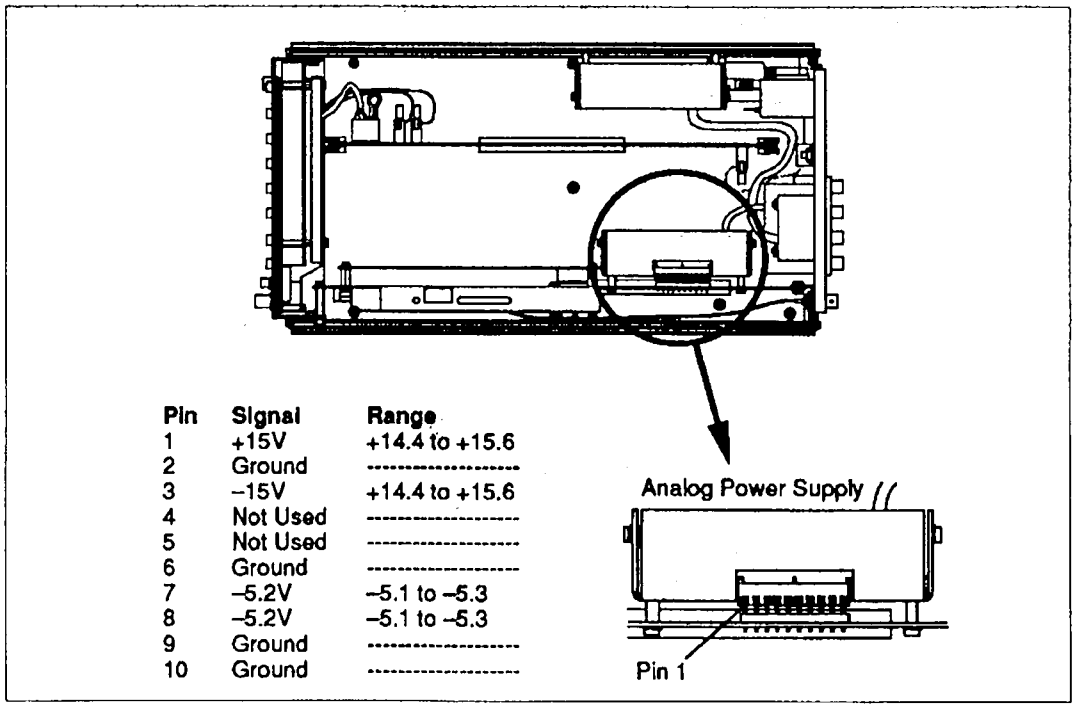
(5) Referring to Figure 4-5, locate the Analog Power Supply connector and measure the voltages using a digital multimeter.

Figure 4-4. Digital Power Supply Test Points



Pin	Signal	Range
1	+15V	+14.4 to +15.6
2	Ground	----------
3	–15V	–14.4 to –15.6
4	+18V	+16.0 to +18.0
5	+5V	+4.9 to +5.1
6	Ground	----------
7	Ground	----------
8	Ground	----------
9	+5V	+4.9 to +5.1
10	+5V	+4.9 to +5.1

Figure 4-5. Analog Power Supply Test Points



Pin	Signal	Range
1	+15V	+14.4 to +15.6
2	Ground	----------
3	–15V	+14.4 to +15.6
4	Not Used	----------
5	Not Used	----------
6	Ground	----------
7	–5.2V	–5.1 to –5.3
8	–5.2V	–5.1 to –5.3
9	Ground	----------
10	Ground	----------

Section 5
Semi-Automatic Calibration

5.1 INTRODUCTION

This section describes a semi-automatic method of calibrating your Multifunction Waveform Synthesizer using a PC and the Calibration Software disk supplied with this manual. The Test Software can communicate with this instrument through either the RS232 or GPIB (IEEE-488) port. If you choose to use the GPIB port, a GPIB card must be installed in the PC before this calibration can be performed.

NOTE: The GPIB card and supporting GPIB software are not supplied with this manual.

5.2 RECOMMENDED TEST EQUIPMENT

- ❑ IBM-PC or compatible
- ❑ HP5334B Frequency counter with Option-01 (oven-stabilized crystal) or equivalent
- ❑ Tektronix Model 2465 High-Speed Oscilloscope with Tektronix 7A22 Differential Input Scope Plug-In or equivalent
- ❑ HP3458A AC-DC Voltmeter or equivalent
- ❑ Non-metallic adjusting tool
- ❑ For GPIB users: National Instruments GPIB Interface card and supporting software (Must be compatible with software driver NI-488.2 from National Instruments)

5.3 CALIBRATION PROGRAM OVERVIEW

The calibration program begins by asking you to select the interface used to communicate with the Unit Under Test (UUT). If using the RS232 port, the program displays its main menu of selections (Figure 5-1). If using the GPIB port, you are ask to enter the device number of the UUT before the main menu is displayed. To use any of these routines, just enter the number of your choice and follow the instructions as they appear on the monitor. Entering zero exits the program.

Figure 5-1. Calibration Program Main Menu Display

```
**********************************************************
MULTIFUNCTION WAVEFORM SYNTHESIZER CALIBRATION PROCEDURE
**********************************************************

 (1) Link Test
 (2) Oscillator Calibration
 (3) Output Amplifier Flatness Calibration
 (4) Converter gain, offset, and zero crossing calibration
 (0) Exit

Enter choice:
```

5.3.1 Link Test (1)

This test is used to check the communications link between the PC to the Unit Under Test (UUT). It is a good idea to run this test after you first power-on the unit.

5.3.2 Oscillator Calibration (2)

This routine allows you to calibrate the internal oscillator and consists of the following adjustments:

- ❑ Internal Reference Oscillator Frequency Calibration
- ❑ Main Oscillator Duty Cycle Calibration
- ❑ Main Oscillator Sideband Minimization
- ❑ Deviation adjustment of Phase Slip Oscillator

These adjustments are performed in order. Following the last adjustment routine, the program returns to the main menu.

5.3.3 Output Amplifier Flatness Calibration (3)

This routine allows you to adjust the flatness specification of the output amplifier. The program returns to the main menu following this routine.

5.3.4 Converter Gain, Offset, and Zero Crossing Calibration (4)

This routine is used to calibrate the DAC output. Perform the following adjustments in order. Following the last adjustment routine, the program returns to the main menu.

- ❑ Offset Errors in the D/A Converter REF INPUT SIGNAL
- ❑ D/A Converter Absolute Gain
- ❑ D/A Converter Offset
- ❑ Offset Generator Full Scale
- ❑ Offset Generator Accuracy Near Zero
- ❑ Offset Generator Zero Point

5.3.5 Exit (0)

Entering 0 exits `cal_test.exe` and returns control to whatever was running before.

5.4 HARDWARE SETUP

5.4.1 For RS232 Communications

(1) Verify that the fuse and voltage settings of the Unit Under Test (UUT) are appropriate for the local AC power.

(2) Connect the UUT to the AC Mains.

(3) Connect the UUT serial port (RS232) to COM1 on your PC.

(4) Set the UUT power to ON and wait for the self tests to run.

(5) Set the UUT to 9600 baud, no parity, 1 stop bit; and transfer control to the RS232 port.

(6) Install the calibration software. Refer to Section 5.5.1.

5.4.2 For GPIB Communications

(1) Install a National Instruments GPIB Interface card in your PC. The GPIB card must be compatible with software driver NI-488.2 from National Instruments.

(2) Verify that the fuse and voltage settings of the Unit Under Test (UUT) are appropriate for the local AC power.

(3) Connect the UUT to the AC Mains.

(4) Connect the UUT GPIB port to the GPIB port of the PC using a standard GPIB cable.

(5) Set the UUT power to ON and wait for the self tests to run.

(6) Install the calibration software. Refer to Section 5.5.2.

5.5 CALIBRATION SOFTWARE INSTALLATION

5.5.1 RS232 Software Installation

For RS232 interfacing, install these two files in your computer system – these files are provided on the Calibration Software disk:

`driver.bin` ....RS232 software driver for the UUT

`cal_test.exe` ..Semi-automatic calibration program

(1) Copy `driver.bin` and `cal_test.exe` to your hard drive.

(2) Add the following line to your `config.sys` file. Make sure that the path to `driver.bin` in `config.sys` is correct. This line may differ from your setting if you copied the driver to a subdirectory on your hard drive.

```
DEVICE=C:\DRIVER.BIN/SPEED=9600/NAME=WAVE/
TIME=100/BUFFER=1000/VERBOSE
```

(3) Reboot your PC.

(4) Run `cal_test.exe` to start the calibration program.

5.5.2 GPIB Software Installation

For GPIB interfacing, install these three files in your computer system – only `cal_test.exe` is provided on the Calibration Software disk, `gpib.com` and `ibconf.exe` can be obtained from National Instruments:

`ibconf.exe` ....Configuration program supplied by National Instruments

`gpib.com` ......GPIB software driver supplied by National Instruments

`cal_test.exe` ..Semi-automatic calibration program from Analogic

(1) Copy `cal_test.exe` to your hard drive from the calibration software disk.

(2) If not previously installed, copy `gpib.com` and `ibconf.exe` to your hard drive from the National disk and reboot your PC.

(3) Run `ibconf.exe` and configure the GPIB interface for the UUT.

(4) Run `cal_test.exe` to start the calibration program.

5.6 SYSTEM CALIBRATION PROCEDURE

Each routine of the calibration program tells you how and when to connect the test equipment and what control to adjust. Therefore, the following is only a general guideline when the actual calibration process begins. Figures are provided to identify the locations of adjustment controls and test points.

NOTE: Allow the UUT to warm up for at least one hour before performing calibration.

(1) Run `cal_test.exe`.

(2) Select RS232 or GPIB on the PC. If GPIB was selected, enter the device number of the UUT (Default = DEV1).

(3) Select the Link Test to verify that the PC is communicating with the UUT.

(4) Remove the Top Cover of the UUT and immediately start the calibration process.

(5) Run the Oscillator Calibration routine (#2) and follow the instructions given by the screen prompts. Refer to Figures 5-2 through 5-5 to locate adjustments and test points.

CAUTION: The adjusting tool must be non-metallic since the oscillator frequency is affected by metal and because AC line voltage is present on nearby terminals.

(6) Run the Output Amplifier Flatness Calibration (#3) routine and follow the instructions given by the screen prompts. Refer to Figure 5-6 to locate the adjustments.

(7) Run Converter Gain, Offset, and Zero Crossing Calibration (#4) routines and follow the instructions given by the screen prompts. Refer to Figure 5-6 to locate the adjustments.

(8) Calibration is complete. Enter zero to exit the Calibration program.

(9) Set the UUT power to OFF and install the Top Cover.

Figure 5-2. Internal Oscillator Adjustment

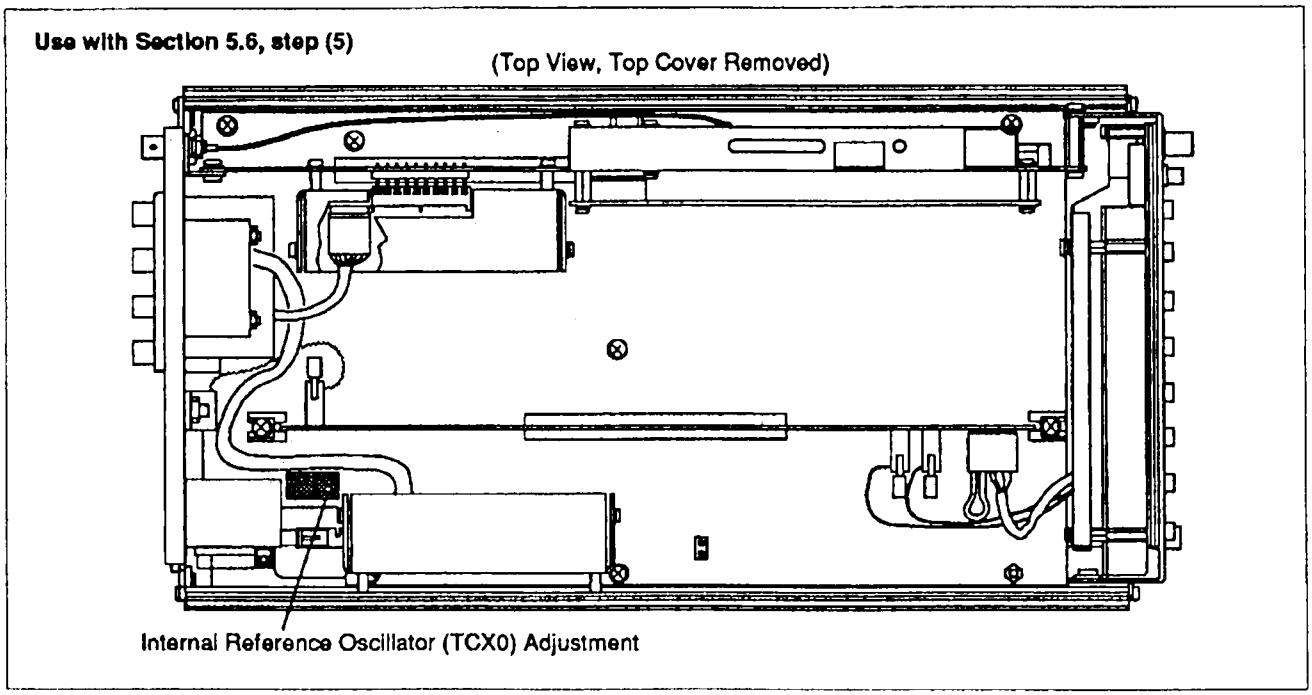


Figure 5-3. Analog Board Test Points 1 and 8

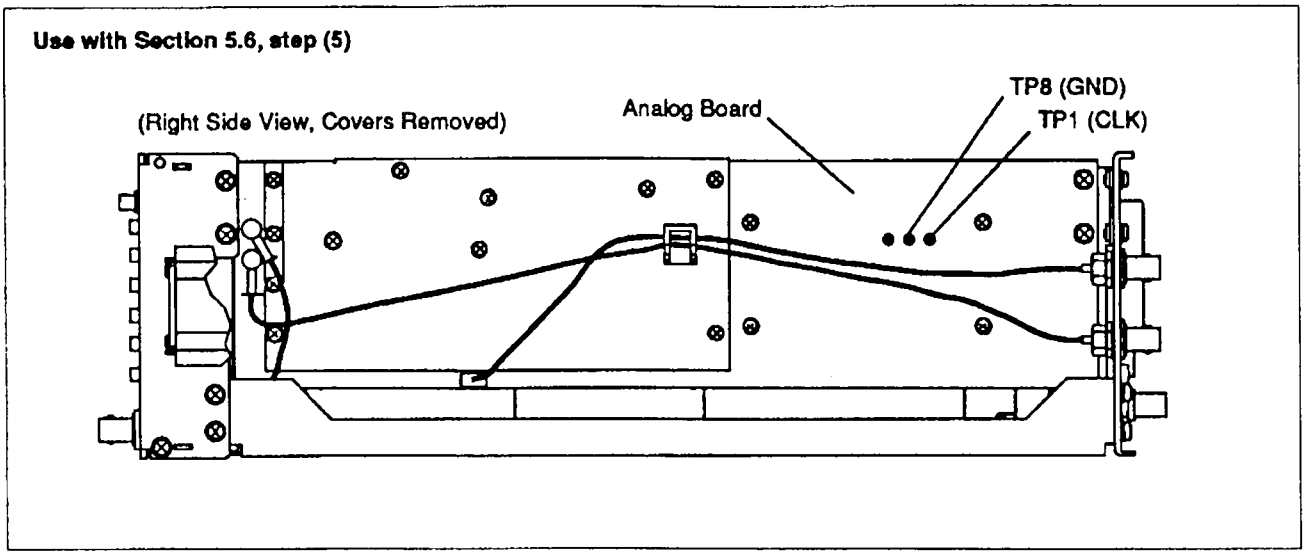


Figure 5-4. DSP Board Adjustments

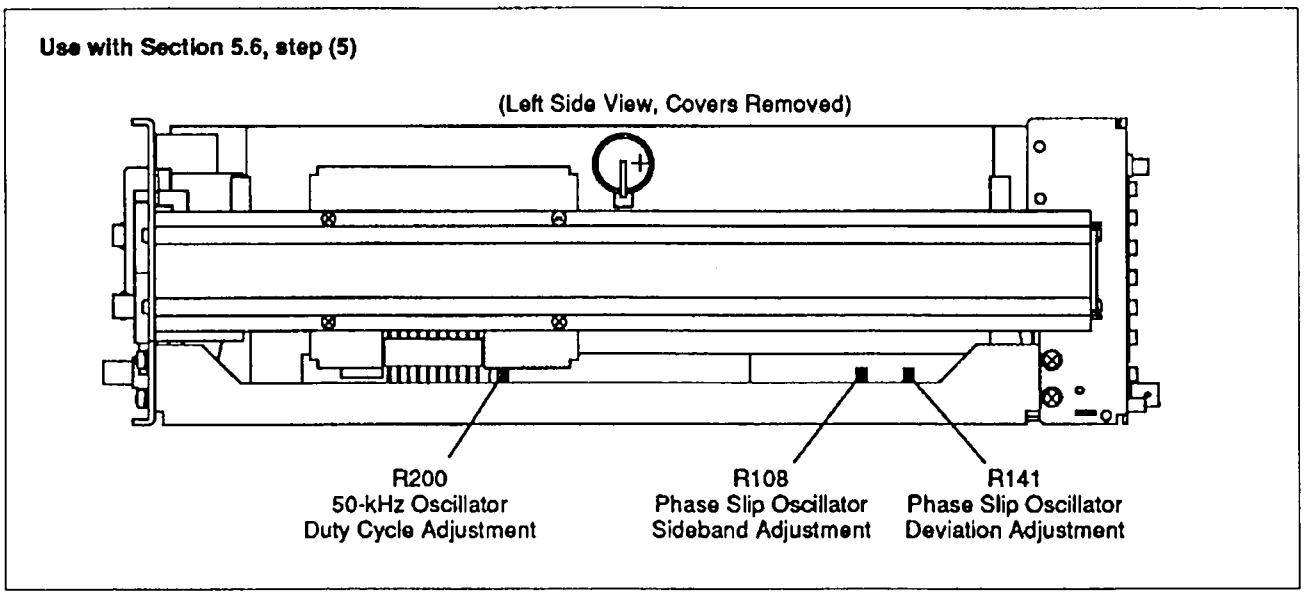


Figure 5-5. Location of JP9

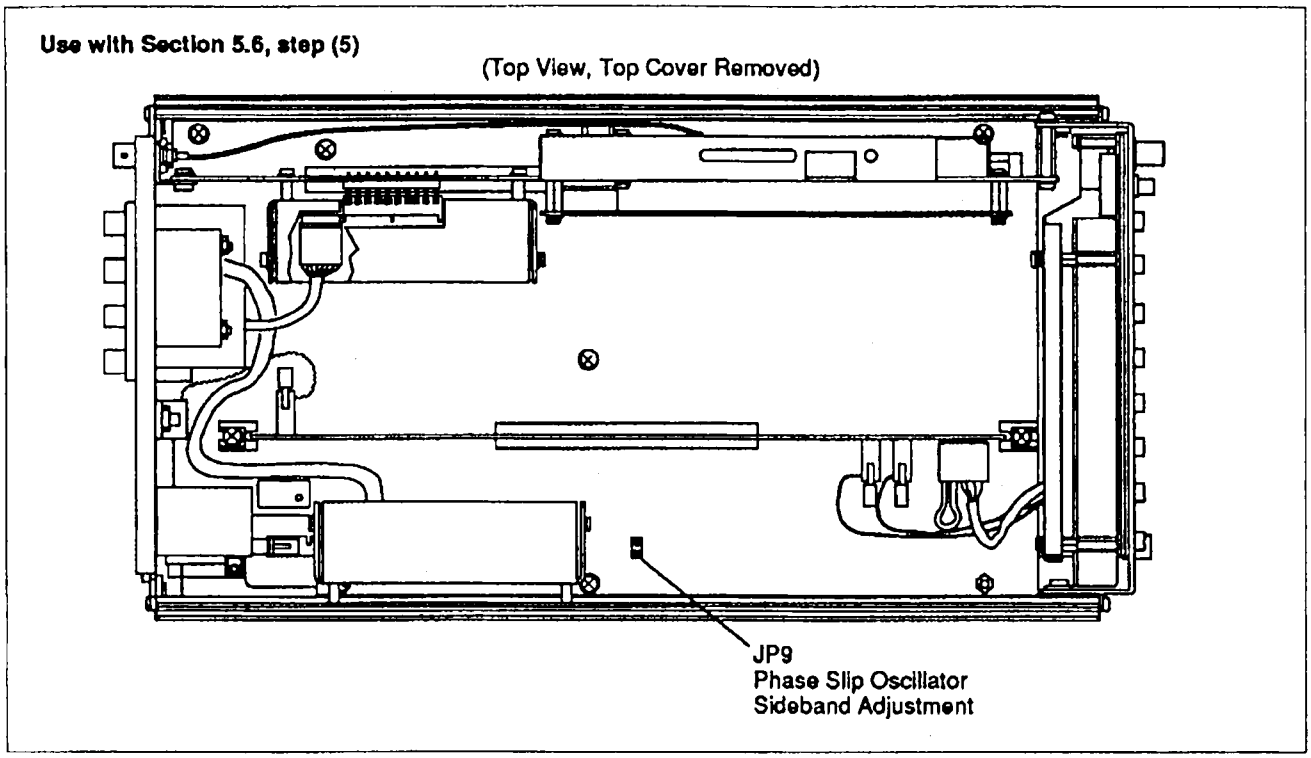
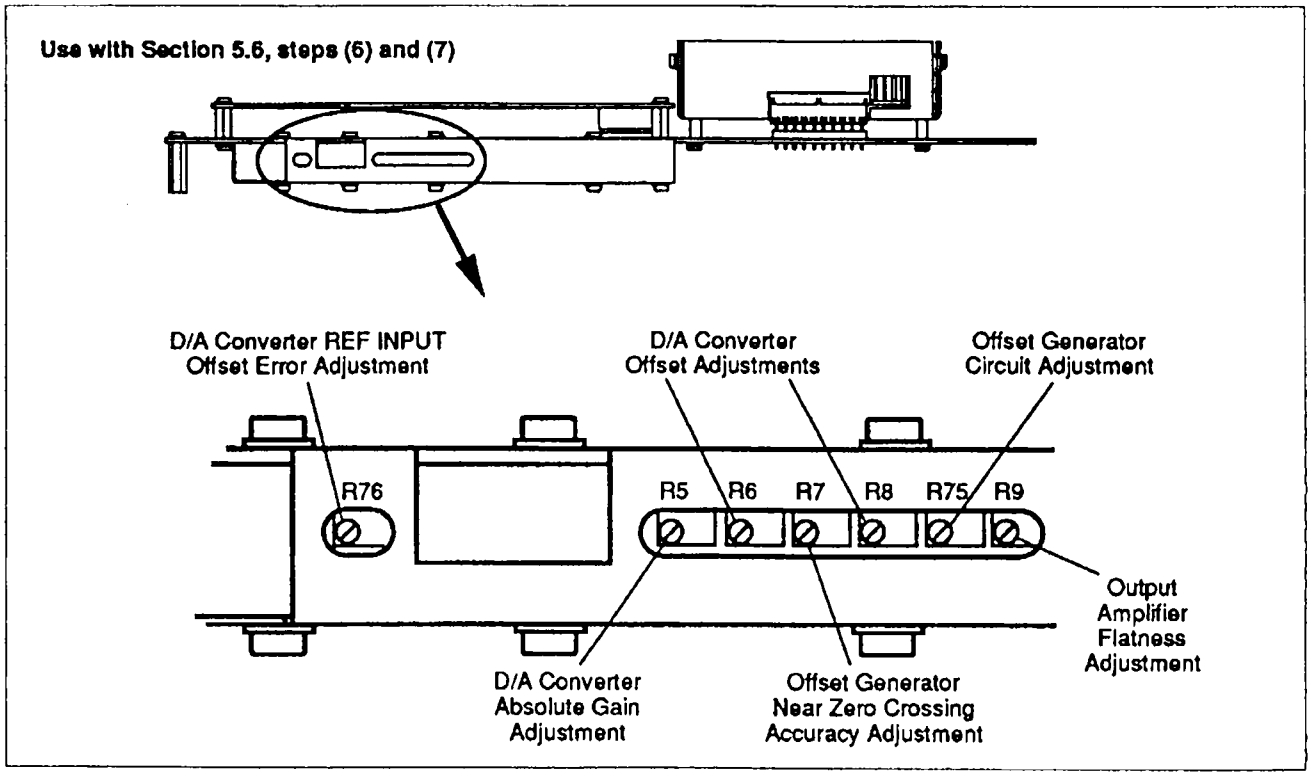


Figure 5-6. Analog Board Adjustments



Section 7
Schematic Diagrams

This section contains the following schematic diagrams:

Name	Drawing No.
CPU Interface	5-11293
DSP-Memory	5-11299
Analog Board	5-11298
Filter Board	5-13909
Front Panel Keyboard	5-13950
Power Supply	5-13907
Primary Side Wiring	5-12572

REVISIONS					
REV	ECO	DESCRIPTION	CHK	ENG	APPLS	DATE
2	N-7643	RELEASED	AR	RD	PS	6-21-91

SIZE D 5-11293 REV 2

CAUTION
THIS ASSEMBLY CONTAINS ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058

RS232 DRIVER

GPIB CONNECTOR

GPIB 488 INTERFACE

NON-VOL BATTERY BACKUP

PAL16L8 BUS DECODER

NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.

LAST REF. DES. USED	REF. DES. NOT USED
BT1, C57, D3, E16, J6, JP21, L1, P1, Q1, R9, RN5, SW1, T1, U39, Y1	E3, J2, J3

PL10-11293 | D2030 | NEXT ASSY | USED ON | APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .X ± .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

DRAWN R. DUDLEY	DATE 31JUL90	
CHECKED L.M.		5-4-91
ENGINEER		5-23-91
ENGINEERING MGR.		5/31/91
QUALITY CONTROL		5/29/91
PRODUCTION		5/31/91
WEIGHT		

ANALOGIC PEABODY, MA. 01960

SCHEMATIC
CPU-INTERFACE
AN2030

CODE IDENT NO. 1BM00 | SIZE D | 5-11293 | REV 2 | SCALE: NONE | SHEET 1 OF 2

14AUG90

REV	ECO	DESCRIPTION	CHK	DWN	APPR'D	DATE
		SEE SHEET 1			PS	5-31-91

D 5-11293 2 REV

WARNING HIGH VOLTAGE

CAUTION THIS ASSEMBLY CONTAINS ELECTROSTATIC SENSITIVE DEVICES HANDLE PER A2-1058

SPARES

CUTTABLE ETCH JP5-JP16

KEYBOARD ENCODER

CONTRAST GENERATOR

LCD DISPLAY

FLOURESENT TUBE DRIVER

SAFETY KEY

WHEEL ENCODER

WHEEL BUFFER

ANALOGIC PEABODY, MA. 01960

CODE IDENT NO.	SIZE		REV
1BM00	D	5-11293	2
SCALE: NONE	CPU-INTERFACE AN2030	SHEET 2 OF 2	

14AU690

NOTES:
1. RESISTANCE VALUES ARE IN OHMS AND ARE 1/4W, 5% CARBON.
2. CAPACITANCE VALUES ARE IN MICROFARADS AND ARE RATED AT 50 VOLTS.

REVISIONS					
REV	ECO	DESCRIPTION	CHK	DWN	APPR'D	DATE
0A	11-8050	RELEASE	RR	DRK	JS	1-2-92
0B	11-8222	SEE E.C.O.	RR	ADM	[illegible]	[illegible]

SIZE D 5-11299 REV 0B

CAUTION THIS ASSEMBLY CONTAINS ELECTROSTATIC SENSITIVE DEVICES HANDLE PER A2-1058

U1 DSP56001 · U2 82C54 · U3 RCT574 · U4 ACT564 · U5 ACT138 · U6 PAL16L8 · U7 PAL16L8 · U8 LF442 · U9 LM361 · U10 32KX8SR · U11 32KX8SR · U12 32KX8SR · U13 ACT74 · U14 ACT74 · U15 ACT74 · U16 GAL16V8 · U17 GAL16V8 · U18 GAL16V8 · U19 ACT138 · U20 F32 · U21 ACT00 · U22 AS878 · U23 HC125 · U40 F08 · U70 ACT74

RN1 1K · RN2 100K 1% · RN3 100K 1% · RN7 100 · RN8 100 · RN9 100

R1 9.09K 1% · R2 1.00K 1% · R3 6.98K 1% · R4 1.62K 1% · R5 110K 1% · R10 100 · R11 100 · R14 200 · R21 1K 5%

C1 6.8 25V · C2 22 25V · C3 22 25V · C4 .1 SPARE · C5 .1 · C6 .1 · C9 .1 · C10 .1 · C11 [illegible] · C12 .1 · C16 .1 · C17 .1 · C18 .1 · C19 .1 · C20 .1 · C22 .1 · C23 .1 · C24 .1 · C25 100pF · C26 .1 · C63 .1 · C75 .1 · C76 .1 · C77 .1 · C78 .1 · C79 .1 · C80 .1 · C81 .1 · C82 .1 · C83 .1 · C84 .1 · C85 .1 · C150 150pF · C151 150pF · C152 150pF · C153 150pF · C154 150pF · C155 150pF · C156 150pF · C157 150pF · C158 150pF · C159 150pF · C160 150pF · C161 150pF

TP1 TP2 TP3 TP4 GND · J1/A1–J1/A36 · J1/B1–J1/B36 · J5/1–J5/10 · JP1 CUTTABLE ETCH · JP2 DSPRST# · JP8 TRIGSTB# · J3 TRIGERIN

V40DATA(0:7) · V40ADDR(0:3) · DATA(0:23) · BADR(0:15) · DLBADR(1:12) · Q(0:4) · I(0:4) · S(0:6) · CLR(0:4) · TRGSRC(0:1) · MARKER#(0:7) · GATETYP(0:2)

WAIT# · IOAD# · IOWR# · OSCLOCK · REFGOOD · HR/W · HEN# · INTB# · HAK# · BLIGHT · CNTEN0# · TRIGSTB# · CLKSEL# · CLKDAC0# · SERSTB0# · SERSTB1# · SERCLK · SERDAT · SOFTTRIG · GET188 · OVERLD# · DSPRST# · DSPRST# · INTA# · DSPCLK · RTINTEN · DX0 · DX1 · DX2 · MODE1 · MODE0 · REALMD · TRIGEN · REINIT · SETONE# · FREERUN · +SP/-SP# · TOSTSP# · STSP# · GTTOST# · VARCLK · TRIGLVL · 5MHZ · RFRSHCLK · BR/WT · BS/BS · RESET · TRQA · TRQB · EXTAL · XTAL · PC3 · PC4 · PC5 · PC6 · PC1 · PC0 · PC2 · PC7 · PC8 · HA0 · HA1 · HA2 · HR/W · HEN · AREQ · HAC · HD0 · HD1 · HD2 · HD3 · HD4 · HD5 · HD6 · HD7 · GND · GND1 · GND2 · GND3 · GND4 · GND5 · GND6 · GND7 · GND8 · GND9 · GND10 · GND11 · GND12 · GND13 · VCC · VCC1 · VCC2 · VCC3 · VCC4 · VCC5 · VCC6 · VCC7 · VCC8 · VCC9 · +5V · +15V · -15V · +5VA · +5VR · +10V · CGND · GND

SPTXFER# · FULXFER# · AURUSTB# · MARKSTB# · CTRSTB# · CLRINT# · SETWAIT# · BADR0 · MODE0 · MODE1 · DATAUR# · AMARD# · SPTXFER# · FULXFER# · DATARD# · TABLEGS# · RESETST# · RUQLSTB# · BDSPLR# · BDSPRD# · PRGSTB# · DATSTB# · X/Y# · BDSPRD# · BDSPLR# · CONFIG · RAMCS# · RAS# · CAS# · DSF · DT#/OE# · WE#/WE# · RAMRD# · DATASTB# · C/ROWE# · WAIT# · XFEREN · XFEREN# · QUEUERU · DSPREST# · BG/WT# · AFRSHCLK · QSFTOGGL · SETWAIT# · BG/WT# · QUEUERU · DATAUR# · DATARD# · BITBOBLE · CTRSTB# · MARKSTB# · 5MHZA · DSPCLK · EXTTRIG · LOWCLK# · UPRCLK# · UPRBCLK# · LOWERE# · UPERERE# · UPERBE# · XFRAST# · QUEUERU

TRIGGER IN FROM REAR PANEL +/-50V MAX.
LEVEL ACCURACY 5% +/-100mV STEPS 100mV
PULSE WIDTH 2x SYSCLK PER MIN, HYSTERESIS 500mV ABOUT THRESH
Rin = 10k 2.5%, Cin < 20pF

LAST REF. DES. USED	REF. DES. NOT USED	REF. DES. NOT USED
C200,JP12,L2,RN8,RT2,J7,U119,D100	C119-C120,C125-C130,C143,C145-149,	R122-R127,R130-R140,R143-R155,
TP1,R216,X2,R188,TC48	C152-C158,C206-249,JP11,RN4-5,U71-	R1-R9, C7,C8,C9,C13,C21,C27.
	U188,D7-D9,R24-36,R115,R118,R119,	C31-C35,C42, C71-C73

PL18-11299 · DP2030 · NEXT ASSY · USED ON · APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .X± .XX± .XXX± ANGLES ±° MATERIAL FINISH APPLICABLE SPECIFICATIONS

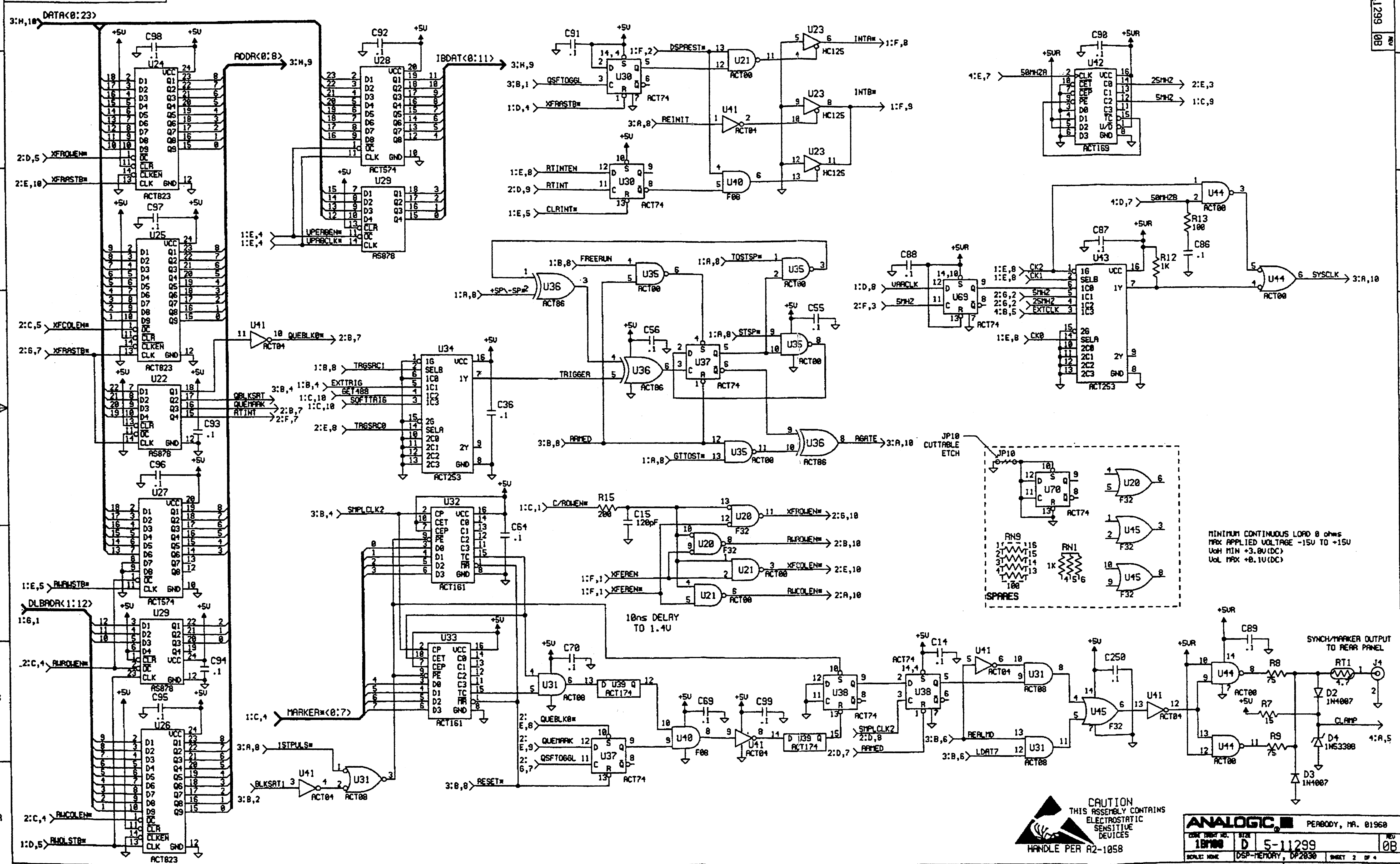
DRAWN	GENE RICHARD	DATE 12/APR/91
CHECKED	R. ROSS	5/26/91
ENGINEER	JEFFREY SAUER	1-2-92
ENGINEERING MGR.	JEFFREY SAUER	1-2-92
QUALITY CONTROL	MIGUEL ALVAREZ	1/3/92
PRODUCTION	S. STREETER	1/3/92
WEIGHT		

ANALOGIC PEABODY, MA. 01960

SCHEMATIC DSP-MEMORY DP2030

CAGE IDENT NO. 18180 · SIZE D · 5-11299 · REV 0B · SCALE: NONE · SHEET 1 OF 4

REVISIONS						
REV	ECO	DESCRIPTION	CHK	DWN	APPLS	DATE
		SEE SHEET 1				



CAUTION
THIS ASSEMBLY CONTAINS ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058

ANALOGIC	PEABODY, MA. 01960		
CODE IDENT NO. 18M00	SIZE D	S-11299	REV 0B
SCALE: NONE	DSP-MEMORY, DP2030	SHEET 2 OF 4	

REVISIONS						
REV	ECO	DESCRIPTION	CHK	DWN	APPR'D	DATE
		SEE SHEET 1				

SIZE D | 5-11299 | REV 08

DATA(0:23)
IBDAT(0:11)
ADDR(0:8)
IRDAT(0:11)
DBDAT(0:11)
LDAT(0:11)
ORDAT(0:11)
D(0:11)
BANKBCLK
BANKACLK
SMPLCLK
SERDAT
SERSTB0#
BUFCLK
SERCLK
SERSTB1#
SMPLCLK2
RESET#
SELECT
OUTPUTCL
CNTRCLK
REALMD
SYSCLK
DLBUFCLK
QSF
QBLKSRT
BLKSRT1
BLKSRT2
OVERLD#
DLBUFCLK
QSFTOGGL
DATASTB#
LOWRCLK#
DATARD#
LOWREN#
UPPRCLK#
UPPREN#
GATETYP(0:2)
RESETST#
AGATE
TRIGEN
BLKSRT2
SYSCLK
BITBOGLE
JP4-JP6 CUTTABLE ETCH
JP7 & JP12 CUTTABLE ETCH
RESET#
ARMED
SDCLKEN#
SMCLKEN#
REINIT
1STPULS#
SPARE
OUTPUTCL

U46 U47 U48 U49 ACT646
U50 U51 U52 U53 U54 U55 MSM44225GL
U56 U57 GAL16V8
U58 AC02
U59 ACT161
U60 GAL20V8
U61 U62 U63 U64 U65 ACT169
U66 U67 U68 F399
U69 ACT74
U36 ACT86
U40 F00
U45 F32
RN5 RN6 RN7 100
C37 C38 C39 C40 C41 C43 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C58 C59 C60 C61 C62 C65 C66 C68 C74 C251 .1
C28 150pF
R16 2.2K
R17 R18 R19 R20 R21 R22 R23 100
R22 R23 75
JP3 JP4 JP5 JP6 JP7 JP12

NOTES:
1. NEED TO GUARANTEE 2 CLOCKS AFTER QSF BEFORE SPLIT TRANSFER.
2. NEED 7 SYSCLOCKS FROM QSF TO STOP WAVE.
3. NEED 6 SYSCLOCKS FROM QSF TO RESTART SYNCH.

CAUTION
THIS ASSEMBLY CONTAINS ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058

ANALOGIC® PEABODY, MA. 01960
DRAWING NO. 18188 | SIZE D | 5-11299 | REV 08
BOILERPLATE | DSP-MEMORY DP2030 | SHEET 3 OF 4

REVISIONS						
REV	ECO	DESCRIPTION	DWN	CHK	APPR	DATE
		SEE SHEET 1				

SIZE D | 5-11299 | REV 08

+15U R117 2K R120 F.R. R121 F.R. C140 15 10U D1 LM336 5V +.01 SVRE6 TO PIN 14 U113 R132 10.00K 0.1% R206 F.A. +/-10V R131 20.0K 1% R141 5K CCW CW +/- 11.25V R103 1.69M 1% R134 510K C109 .33 U103 DG211 2.52V/SEC/PPM R130 10.00K 0.1% R102 160K C102 .47 C131 .047 C254 .01 C253 .01 U104 LF442N BEND 4:F,10 R128 8.06K 1% C104 .01 R129 2.00K 1% R106 10K R111 100K R105 47K R104 100 R108 50K SIDE BANDS C141 .1 U117 HC574 C133 .1 U101 DAC8800 R101 5.00K 0.1% R203 5.1K C101 .01 C134 .1 C108 .22 R107 47K U108 HC123 R214 100K C256 35U U118 HC132 OSCLOCK 1:F,10 1:D,10 CLKDAC0= 4:C,7 V40DATA<0:7> U102 LF442N U103 DG211 R112 10K

BEND 4:B,2 R211 2K C255 1000pF JP9 L2 1.5uH R209 100K C259 10pF D100 MV209 VCC R207 220 C202 .01 X1 50MHZ R210 10K C205 120pF L1 .1uH SEE NOTE 3 C260 33pF C204 .01 Q100 MPS918 C200 47pF C199 1000pF U116 AC04 R212 1.5K R204 1K C201 1000pF AGND R205 10K C203 0.1 U119 LF442N R200 5K CCW R201 1K 1% R208 100K R202 2.49K 1% U116 50MHZA 1:B,4 50MHZB 2:F,3 C100 .1 C135 .1 U105 ACT169 C136 .1 U106 ACT169 1MHZ C115 .1 U110 HC74 U114 C04 U113 HC00 C138 .1 R109 10K C103 .01 R110 100K U111 HC86 C139 .1 C116 .1 SUREG C258 47pF R216 68 U107 1MHZ-REF C114 .1 R213 10K C257 2200pF U108 HC123 REFGOOD 1:F,10

U112 HC574 U40DATA<0:7> 1:6,8 CLKSEL= 1:D,10 C137 .1 U109 HC00 EXTCLK 2:E,3 C112 .1 C113 .1 U115 HC00 HC132 U118 R136 68 R135 68 REF_FREQ D6 1N4007 D5 1N4007 RT2 J7 CLAMP 2:B,1 C117 .1 J6 EX_FREQ AGND R137 100K R142 20K C142 100pF

C122 47pF X2 10MHz R215 1.2K 5% C121 150pF R116 1M C124 33pF C123 2-22PF TGND VCC1 TCX0 10MHZ (OPTION) C252 .01 FOR OPTION TCX8: REMOVE C121,C122,C123 C124, X2, R116.

C107 15 10U C113 10 C114 10 VCC C111 15 10U C110 15 10U EGND TGND +5U +15U +5VR C105 6.8 20U C144 15 10U C106 6.8 20U AGND -15U R100 0 R133 0 R99 0 EGND TGND

SPARES U119 LF442N U109 HC00 U111 HC86 U114 C04 U115 HC00 U116 AC04

NOTES:
1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS AND ARE RATED AT 50 VOLTS.
3. IF 'BEND' VOLTAGE, MEASURED ON JP9, IS < -12 VOLTS THEN CUT OFF C259. IF IT IS STILL < -12 VOLT CUT OFF C260.

CAUTION THIS ASSEMBLY CONTAINS ELECTROSTATIC SENSITIVE DEVICES HANDLE PER A2-1058

ANALOGIC PEABODY, MA. 01960
CODE IDENT NO. 18000 | SIZE D | 5-11299 | REV 08
SCALE: NONE | DSP-MEMORY D2030 | SHEET 4 OF 4

REVISION

REV	ECO	DESCRIPTION	CHK	DWN	APLS	DATE
2	11-7643	RELEASED	RR	RD	CG	5/31/91
2A	11-7834	SEE E.C.O.	RR	RM	CG	10-2-91
2B	11-8040	DOES NOT EXIST				
2C	11-8040	SEE E.C.O.	RR	RM	CG	1/11/92
2D	11-8221	SEE E.C.O.	RR	DRK	CG	4/10/92

SIZE D 5-11298 REV 2D

VERNIER AMPLITUDE CONTROL

OFFSET GENERATOR

OFFSET GAIN

OFFSET BALANCE

OFFSET ZERO

OUTPUT OVERLOAD DETECTOR (174 mA CURRENT DETECT)

OUTPUT DRIVER

ATTENUATOR 6.020B 12.040B 24.080B 24.080B

EXT MOD

DIGITAL CONNECTOR

FLOATING POWER CONNECTOR

SERIAL - PARALLEL CONVERTER

POWER ON/OFF DISCONNECT

SPARES

NOTES:
1. RESISTANCE VALUES ARE IN OHMS AND ARE 1/4W, 5% UNLESS OTHERWISE NOTED.
2. CAPACITANCE VALUES ARE IN MICROFARADS AND ARE 50 VOLTS.
3. THESE SYMBOLS INDICATE SEPARATE GROUND PLANE, WHICH IS NOT RELATED TO OR CONNECTED TO ANY OTHER GROUNDS.
4. COMPONENT NOT USED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS ANGLES	DRAWN RICH DUDLEY	DATE 2 FEB 90
MATERIAL	CHECKED A.ROSS	5/22/91
	ENGINEER C.BYLES	5/31/91
	ENGINEERING MGR J.SAUER	5/31/91
PL10-11298 2030	QUALITY CONTROL M.ALVAREZ	5/24/91
APPLICATION SPECIFICATIONS	PRODUCTION D.FRADY	5/24/91
APPLICATION	WEIGHT	

ANALOGIC® PEABODY, MA. 01960

SCHEMATIC
ANALOG BOARD
2030

CODE IDENT NO.	SIZE		REV
1BM00	D	5-11298	2D
SCALE:NONE	FILENAME:11298201.SCH		SHEET 1 OF 1

REVISIONS						
REV	ECO	DESCRIPTION	CHK	DWN	APPR	DATE
1		NEW DESIGN		PSB		5/24/90
2	11-7643	RELEASED	RR	JPK	CG	5-31-91
2A	11-8229	SEE E.C.O.	RR	RDM	CG	6/6/91

SIZE D | 5-13909 | REV 2A

100 KHZ FILTER

T1 FILT-IN, GND
T2 FILT-OUT, GND
+12A
MR1*
MR2*
LA*
MED
-12A
J3 20, 18, 16, 14, 12, 10, 8, 6, 4, 2, 19, 17, 15, 13, 11, 9, 7, 5, 3, 1
K1
K2
K3
C1 1000pF
C2 10PF
C3 .033 2%
C4 NOT_USED
C5 1200p 2%
C6 NOT_USED
C7 .056 2%
C8 NOT_USED
C9 2700pf 2%
C10 130pf 5%
C11 .033 2%
C12 NOT_USED
R1 0.33 1W
L10 3.3uh
L1 102uh
L2 102uh

1MHz FILTER

L11 0.22uh
L3 9uh
L4 9uh
C13 1000pF
C14 1000pF
C15 2200pF
C16 82pF
C17 4700pF
C18 180pF
C19 2200pF
C20 1000pF
R3 100K
R4 1M
R5 0.15 1W
SD213
Q1

AMPLITUDE EQUALIZER

C32 NOT_USED
C33 200pF
C34 160pF
C35 90pF
C36 82pF
C37 90pF
R6 88.7 RNS5C 1%
R7 35.7 RNSSC 0.1%
R8 147 RNSSC 1%
R9 150 RNSSC 1%
L12 0.27uh
L13 0.39uh

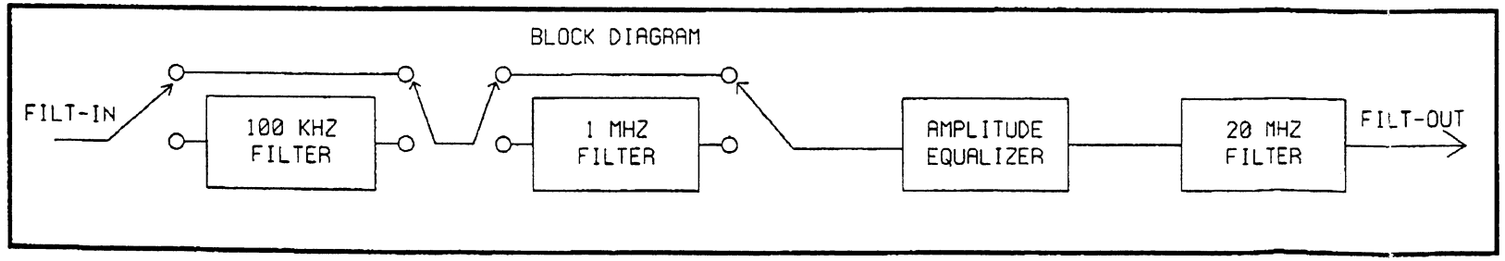
20 MHz FILTER

L5 0.33uh
L6 0.33uh
L7 0.22uh
L8 0.22un
L9 0.33uh
C21 120pF
C22 12pF
C23 200pF
C24 75pF
C25 150pF
C26 150pF
C27 120pF
C28 150pF
C29 160pF
C30 47pF
C31 100pF

MTG1, MTG2, MTG3, MTG4, GND

LAST REF. DES. USED	REF. DES. NOT USED
Q1 C37 R9 K3	R2
L13 T2	

BLOCK DIAGRAM



NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. GROUNDED MOUNTING HOLES

CAUTION
THIS ASSEMBLY CONTAINS ELECTROSTATIC SENSITIVE DEVICES
HANDLE PER A2-1058

PL10-13909	AN2030	DRAWN	P.BITCHELL 5/24/90
NEXT ASSY	USED ON	CHECKED	R Ross 5 3 9
APPLICATION		ENGINEER	J SYLES 5/30/91
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .XX ±.02 .XXX ±.005 ANGLES ±0°		ENGINEERING MGR.	JEFFREY LYLES 5/31/91
MATERIAL		QUALITY CONTROL	MIKE ALVAREZ 5/31/91
FINISH		PRODUCTION	M. PARK... 5/31/91
APPLICABLE SPECIFICATIONS		WEIGHT	

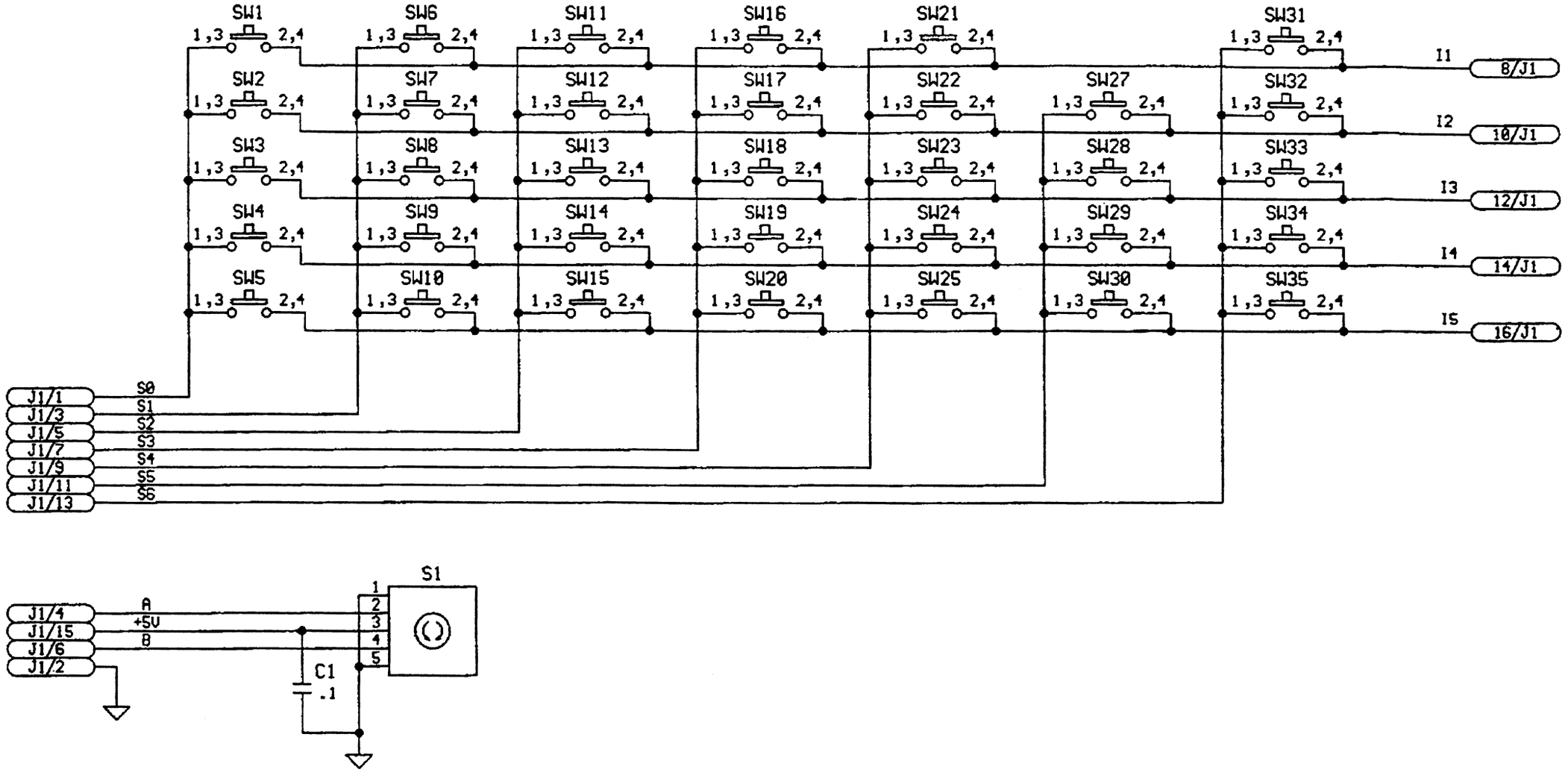
ANALOGIC® PEABODY, MA. 01960

SCHEMATIC
2030 FILTER BOARD

CODE IDENT NO.	SIZE		REV
18H00	D	5-13909	2A
SCALE: NONE		SHEET 1 OF 1	

REVISIONS						
REV	ECO	DESCRIPTION	CHK	DWN	APPLS	DATE
1	11-7581	RELEASE	RR	R.D.	GB	5-1-91

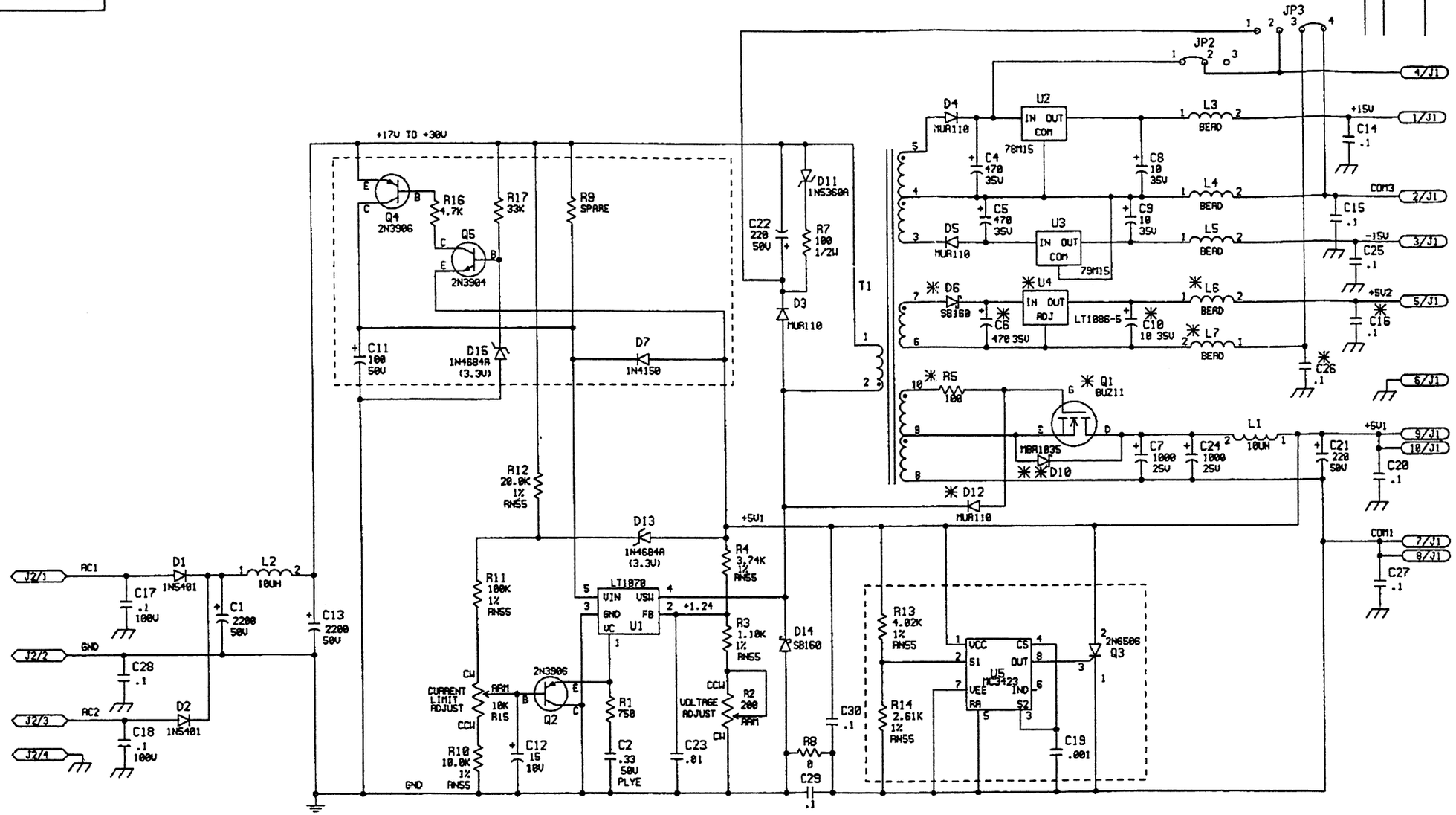
SIZE C | 5-13950 | REV 1

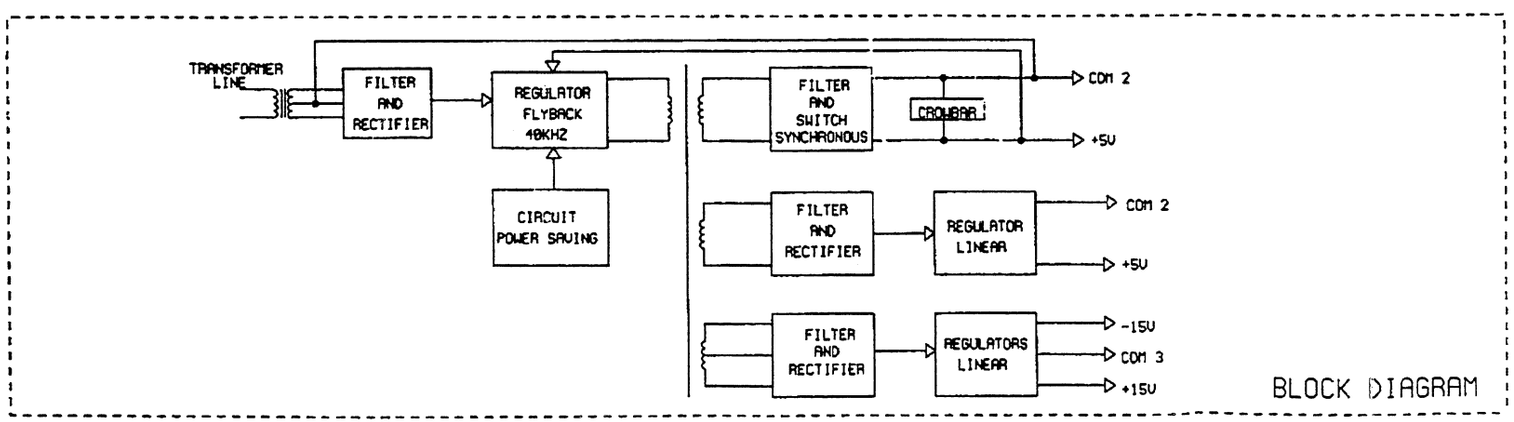


		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .Xx ± .01 .XXx ± .005 ANGLES .XXXx ± 1°	DRAWN GENE RICHARD	DATE 03/15/90	ANALOGIC® PEABODY, MA. 01960
			CHECKED	4/19/91	SCHEMATIC FRONT PANEL KEYBOARD MODEL 2030
		MATERIAL	ENGINEER	4-18-91	
			ENGINEERING MGR.	4-18-91	
		FINISH	QUALITY CONTROL	4/19/91	
PL10-13950	2030		PRODUCTION	4/23/91	
NEXT ASSY	USED ON	APPLICABLE SPECIFICATIONS	WEIGHT		CODE IDENT NO. 18100 / SIZE C / 5-13950 / REV 1
APPLICATION					SCALE: NONE / 13950S11.SCH / SHEET 1 OF 1

REVISIONS						
REV	ECO	DESCRIPTION	CHK	DWN	APPLS	DATE
2	11-7581	RELEASE		MAF		5-1-91

SIZE D 5-13907 REV 2





BLOCK DIAGRAM

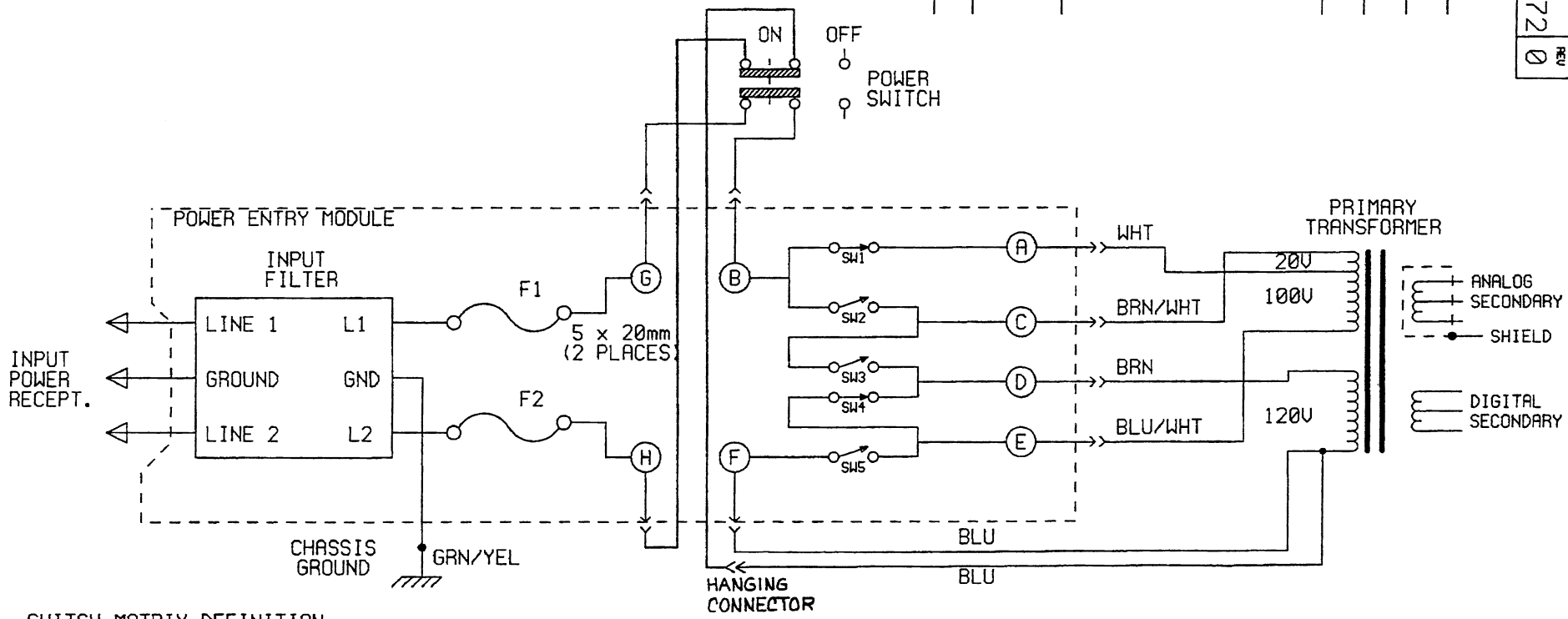
NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS AND ARE 1/4W, 5% CARBON.
2. CAPACITANCE VALUES ARE IN MICROFARADS. CAPACITORS RATED FOR 50V.
3. * DENOTES COMPONENTS INSTALLED PER PL10-13907-001 ONLY.
4. ** DENOTES COMPONENTS INSTALLED PER PL10-13907-002 ONLY.

PL10-13907	AN2030	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .X± .XX± ANGLES .XXX±	DRAWN R.DUDLEY	DATE 2-20-91	ANALOGIC PEABODY, MA. 01960
NEXT ASSY	USED ON	MATERIAL	CHECKED L.RUSSELL	3-13-91	SCHEMATIC POWER SUPPLY 2030
APPLICATION		FINISH	ENGINEER	4-12-91	
		APPLICABLE SPECIFICATIONS	ENGINEERING MGR.	4-12-91	
			QUALITY CONTROL	4/19/91	
			PRODUCTION	4/19/91	
			WEIGHT		CODE IDENT NO. 18M00 / SIZE D / 5-13907 / REV 2
					SCALE: NONE / SHEET 1 OF 1

REVISIONS

REV	ECO	DESCRIPTION	CHK	DWN	APPLS	DATE
0	11-8251	NEW RELEASE	RR	AM	[illegible]	5-13-92

SIZE B 5-12572 REV 0



SWITCH MATRIX DEFINITION

VOLTS	SW1	SW2	SW3	SW4	SW5
100	ON	—	ON	—	ON
120	—	ON	ON	—	ON
220	ON	—	—	ON	—
240	—	ON	—	ON	—

PL10-24471	AN2030
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .X± .XX± .XXX±
ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS

		DATE
DRAWN	JEFFERY SAUER	3-29-92
CHECKED	[signature]	4/10/92
ENGINEER	[signature]	5-13-92
ENGINEERING MGR.	[signature]	5-13-92
QUALITY CONTROL	[signature]	4/10/92
PRODUCTION	[signature]	4-10-92
WEIGHT		

ANALOGIC® PEABODY, MA. 01960

SCHEMATIC

AN2030 PRIMARY SIDE WIRING

CODE IDENT NO.	SIZE		REV
1BM00	B	5-12572	0
SCALE: NONE	FILE NAME: 1257201.SCH	SHEET 1 OF 1	

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