crown

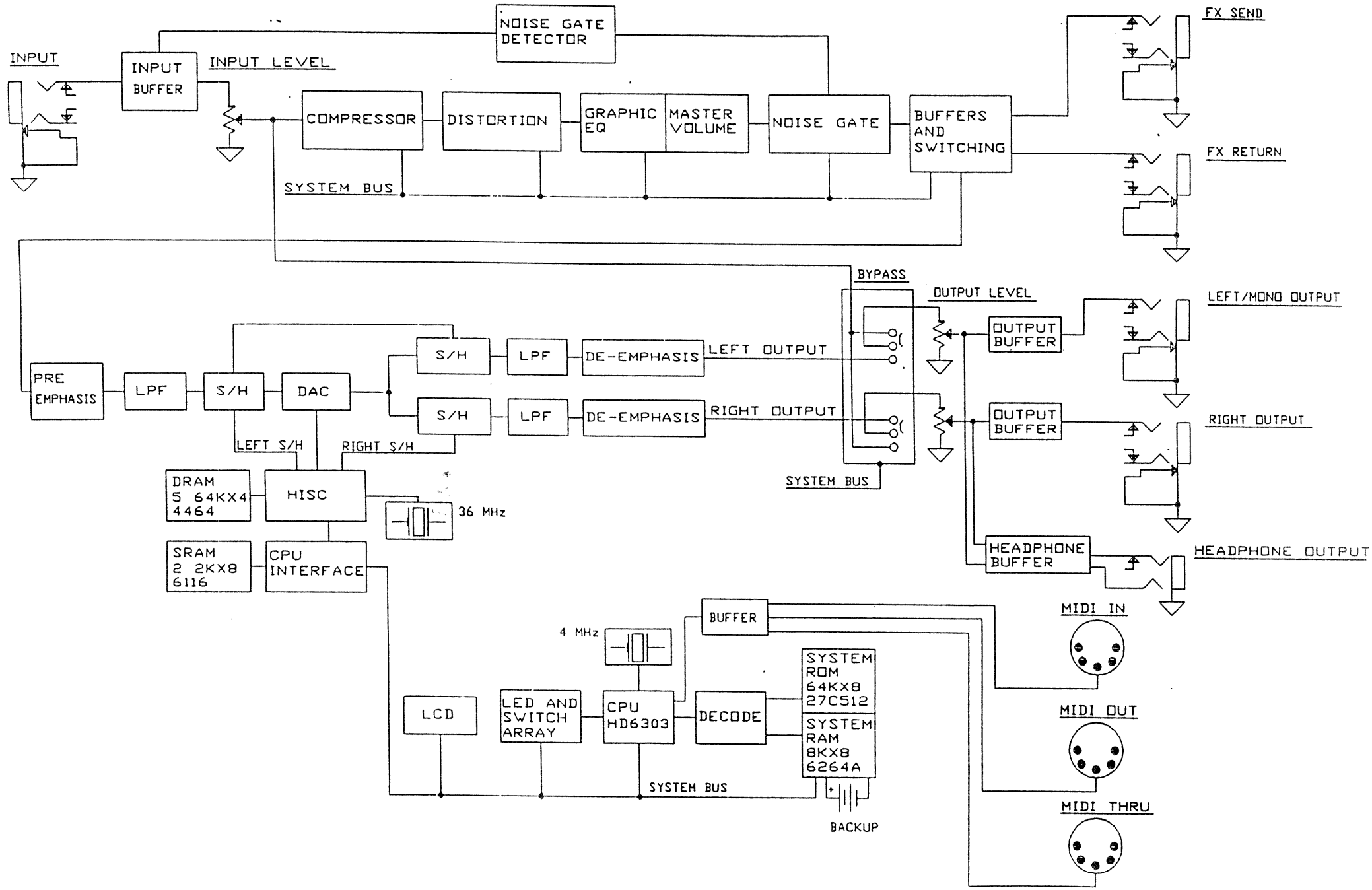
RP-1

Service Manual

- BLOCK DIAGRAM
- SETUP PROCEDURES
- SCHEMATIC DIAGRAMS
- PARTS LISTS
- PC BOARDS
- HISC PINOUT
- HISC PIN DESCRIPTIONS

A Harman International Company

RP4 BLOCK DIAGRAM



RP-1 Setup and Test Procedures

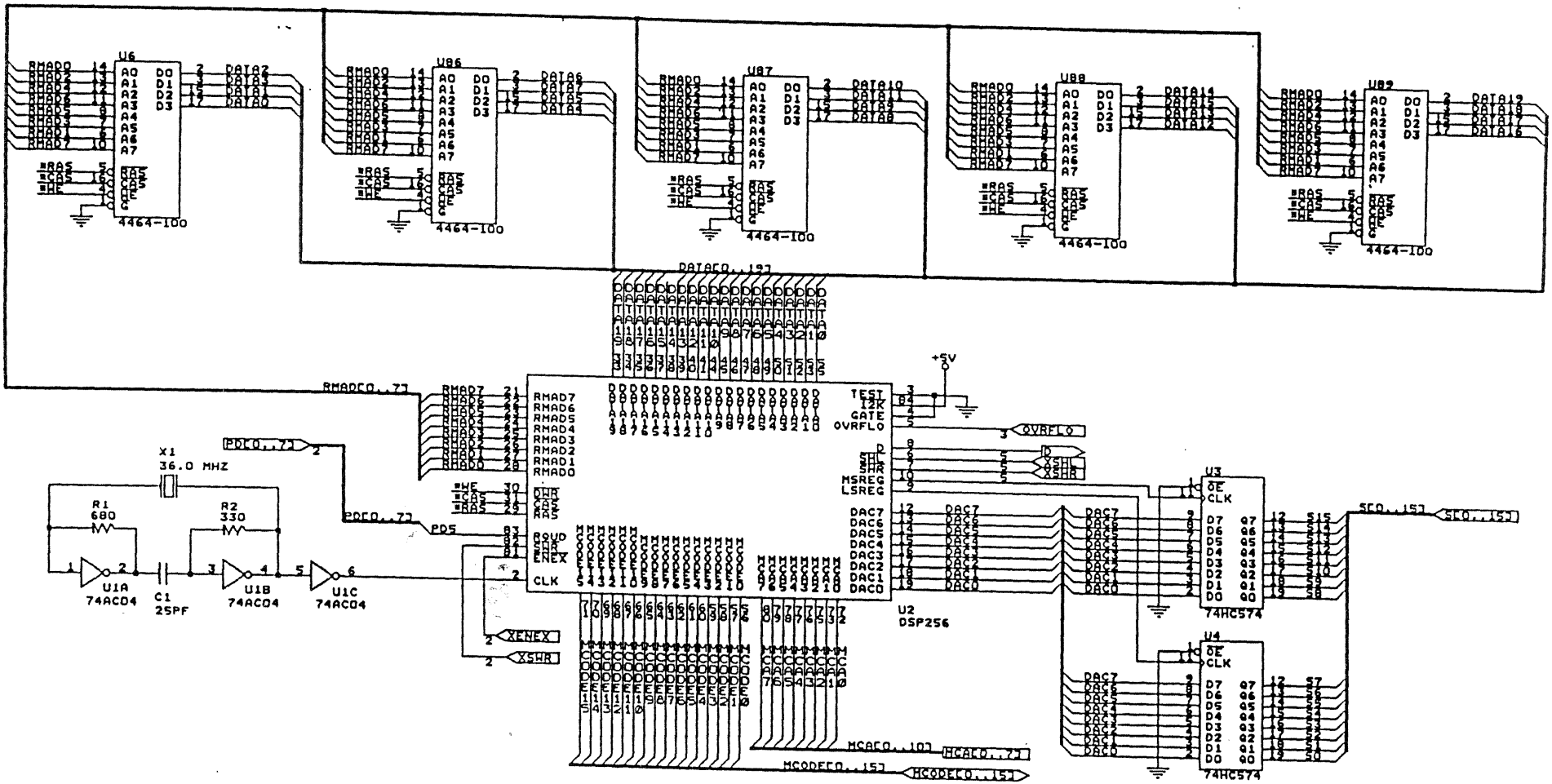
To access the RP-1 setup and test menus, enter the UTILITY mode and scroll left or right until the software version number is displayed. Press the parameter down button twice to enter the test menu. Scroll right to access the compressor gain trim, distortion gain trim, and A/D calibration programs. The procedures for these setup routines are detailed below. Further scrolling will show the EQ test, speaker simulator test, compression test, distortion test, noise gate test, HISC test, RAM test, and display tests. When done, return to the main utility menu.

1. Compressor gain trim: With a 1 Vp-p, 1 KHz sine wave measured at test point one (TP1) on the main PCB, adjust P6 (50K trimpot) until the signal measured at TP4 is the same amplitude as the signal at TP1.

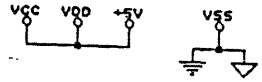
2. Distortion gain trim: Adjust P7 (50k trimpot) until the voltage measured at pin 7 of U97 is between -3mV DC and +3mV DC.

3. A/D Calibration a) Gain: With a 14 Vp-p, 1KHz sine wave measured at TP2, adjust P2 (10K trimpot) until the signal measured at TP3 is 14 Vp-p.

   b) Bias: Reduce the signal level 50 dB to 44.3 mVp-p and adjust P3 (50K trimpot) until the signal seen at TP3 is just barely all positive going or all negative going.



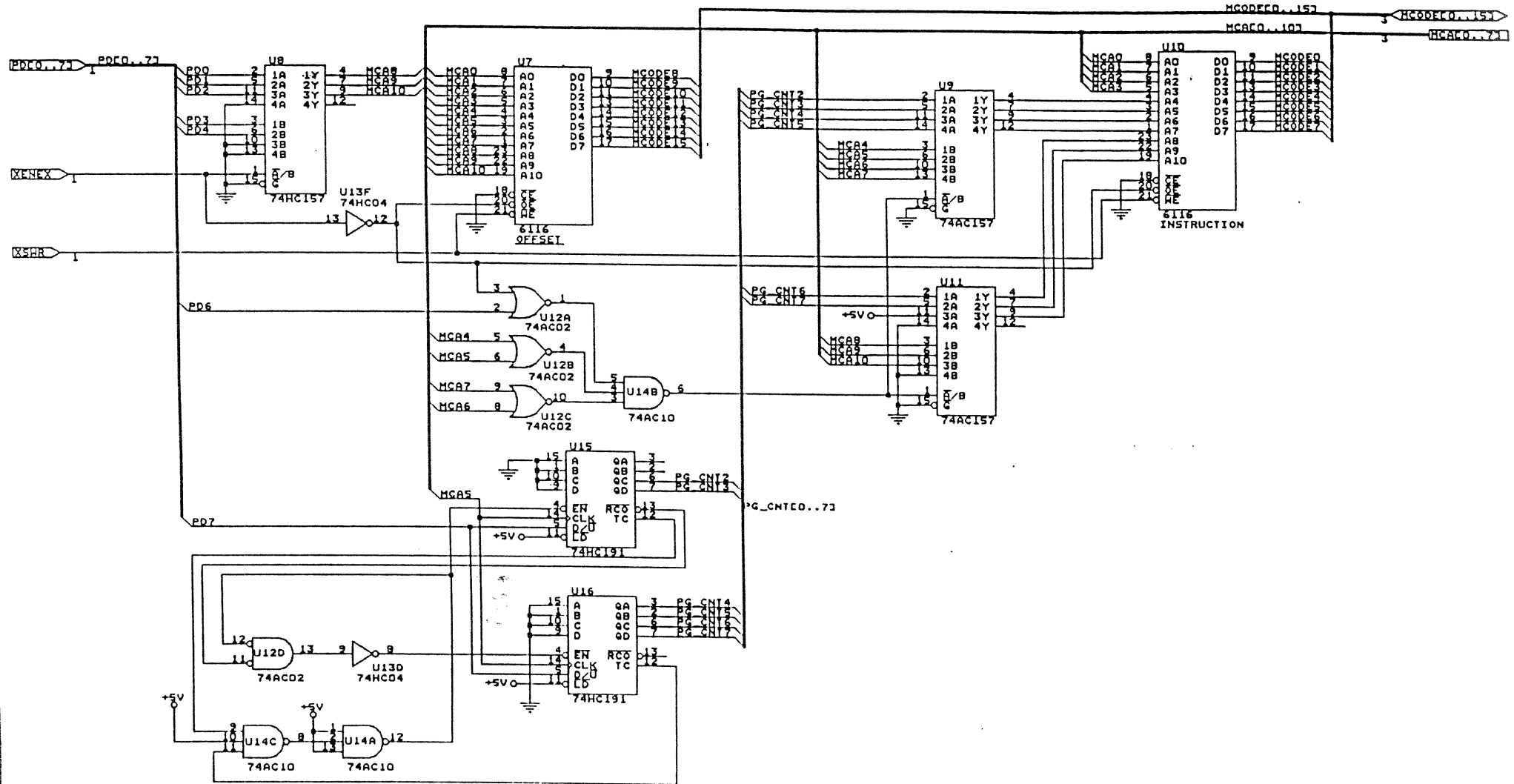
!LINK
!RP1MA801.SCH
!RP1MA802.SCH
!RP1MA803.SCH
!RP1MA804.SCH
!RP1MA805.SCH
!RP1MA806.SCH
!RP1MA807.SCH
!RP1MA808.SCH
!RP1MA809.SCH
!RP1MA780.SCH



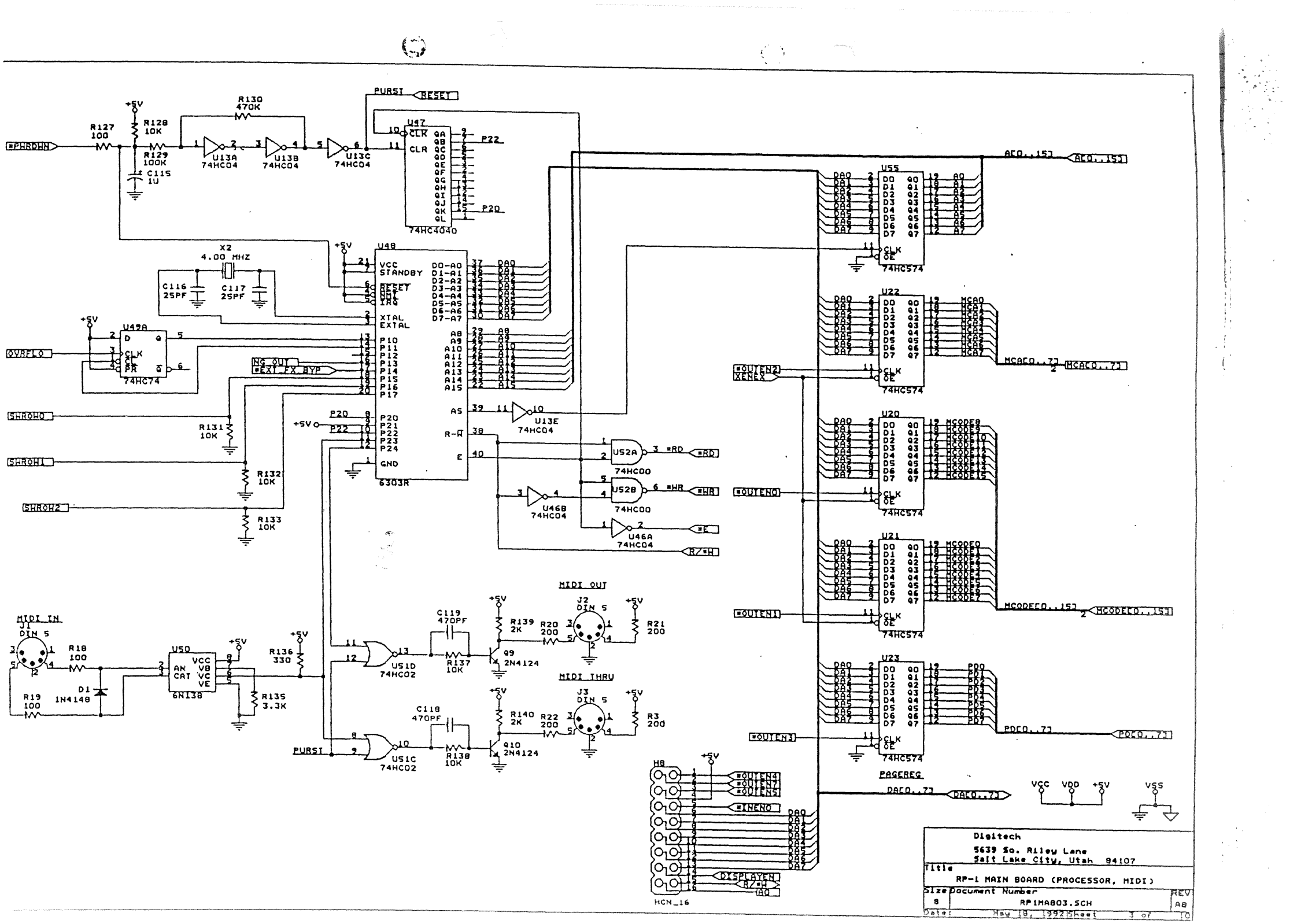
DOD Electronics Inc.
5639 So. Riley Lane
Salt Lake City, Utah 84107

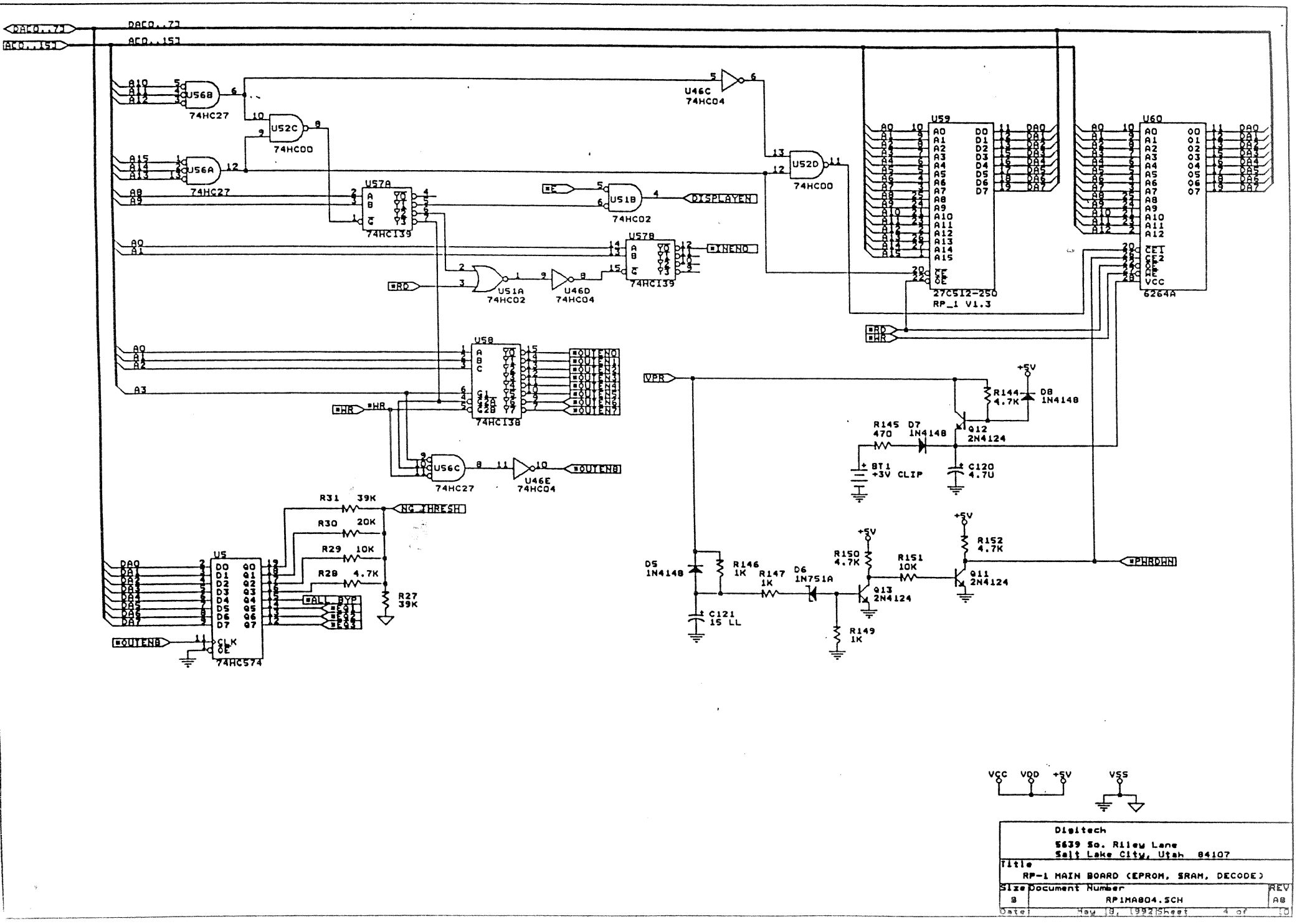
Title
RP-1 MAIN BOARD (HISC SECTION)

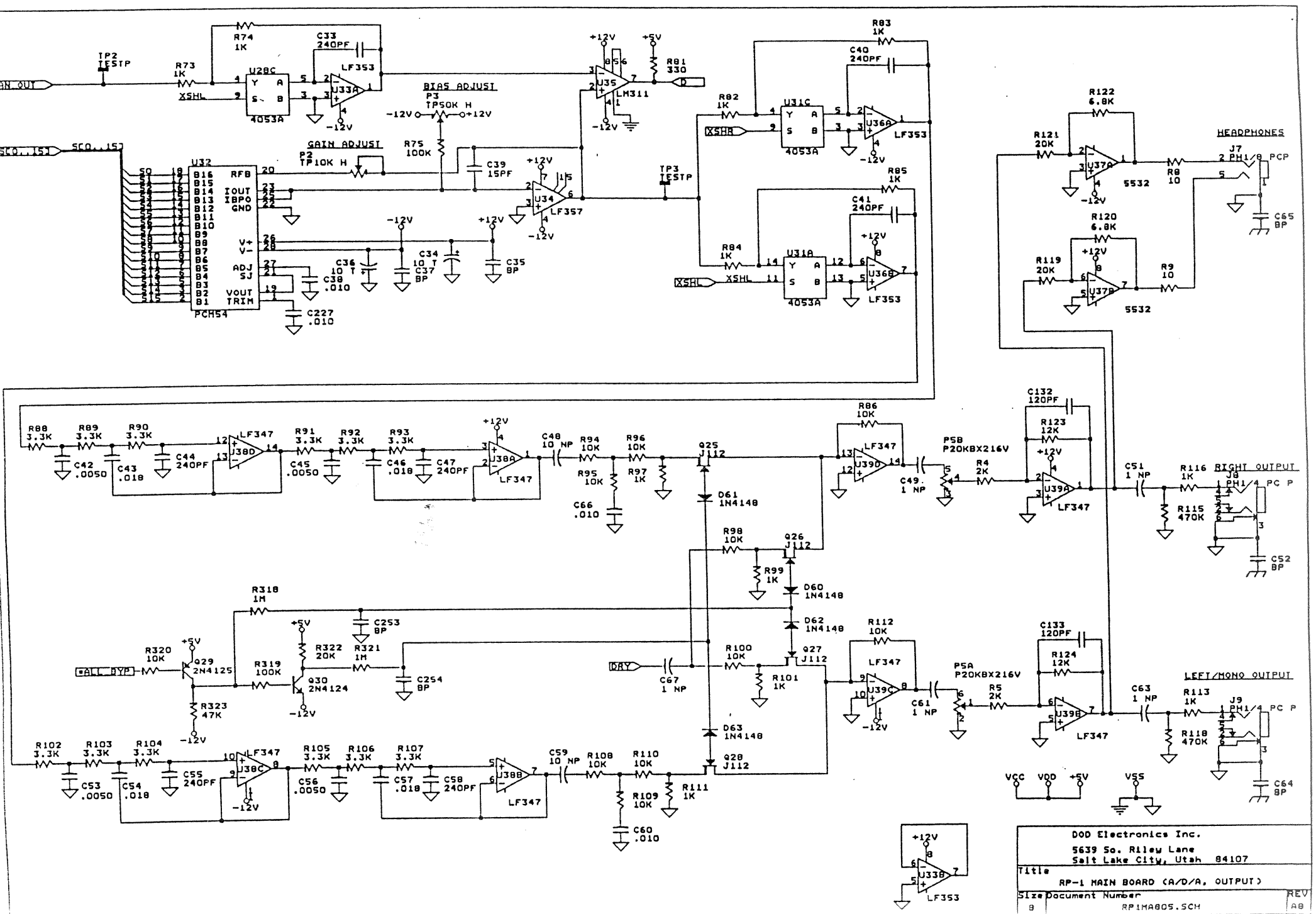
Size Document Number REV

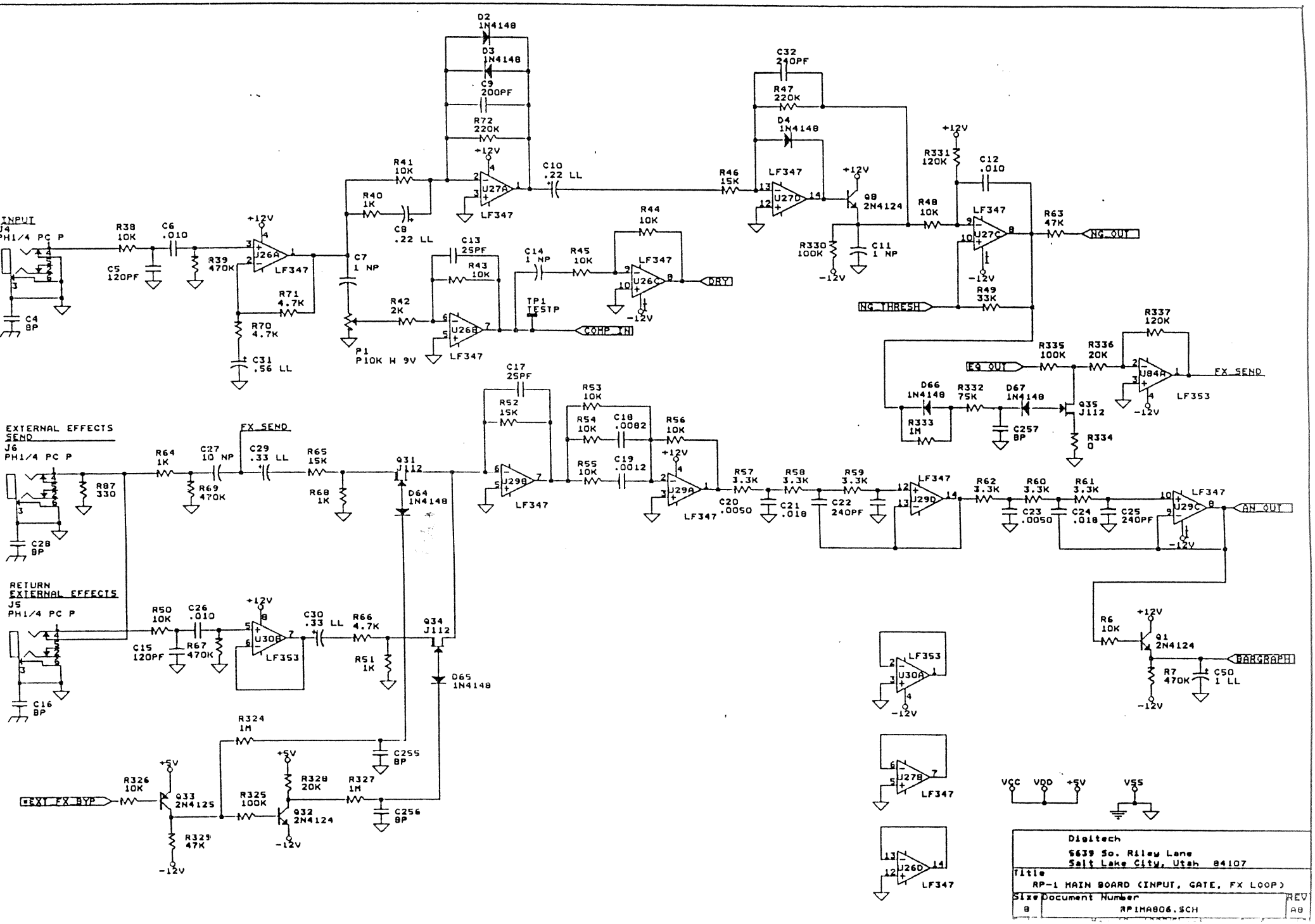


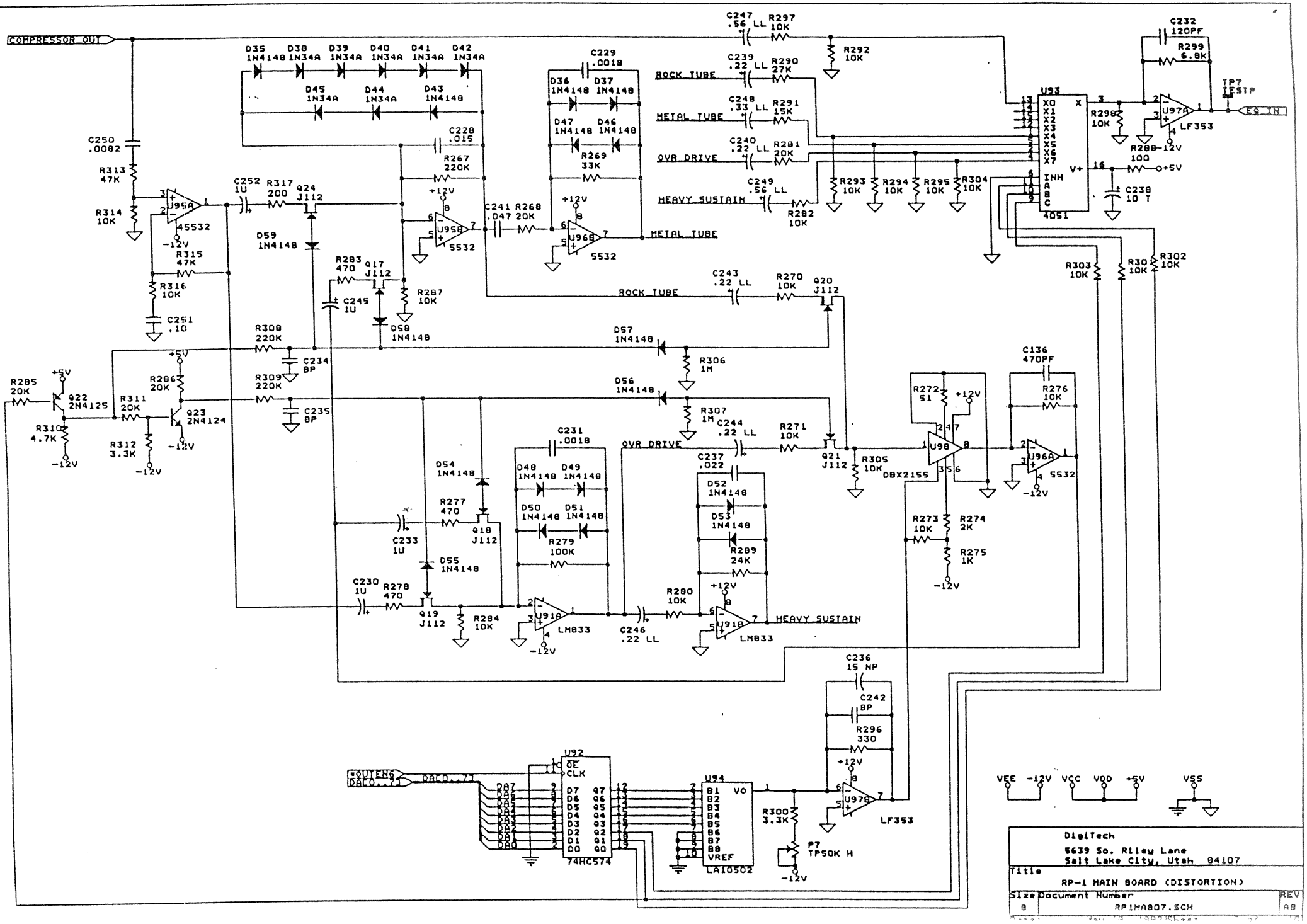
Digitech 5639 So. Riley Lane Salt Lake City, Utah 84107		
Title RP-1 MAIN BOARD (UPDATE AND INST. REG)		
Size B	Document Number RP1MA802.SCH	REV A8
Date: May 19, 1992	Sheet 2 of 10	

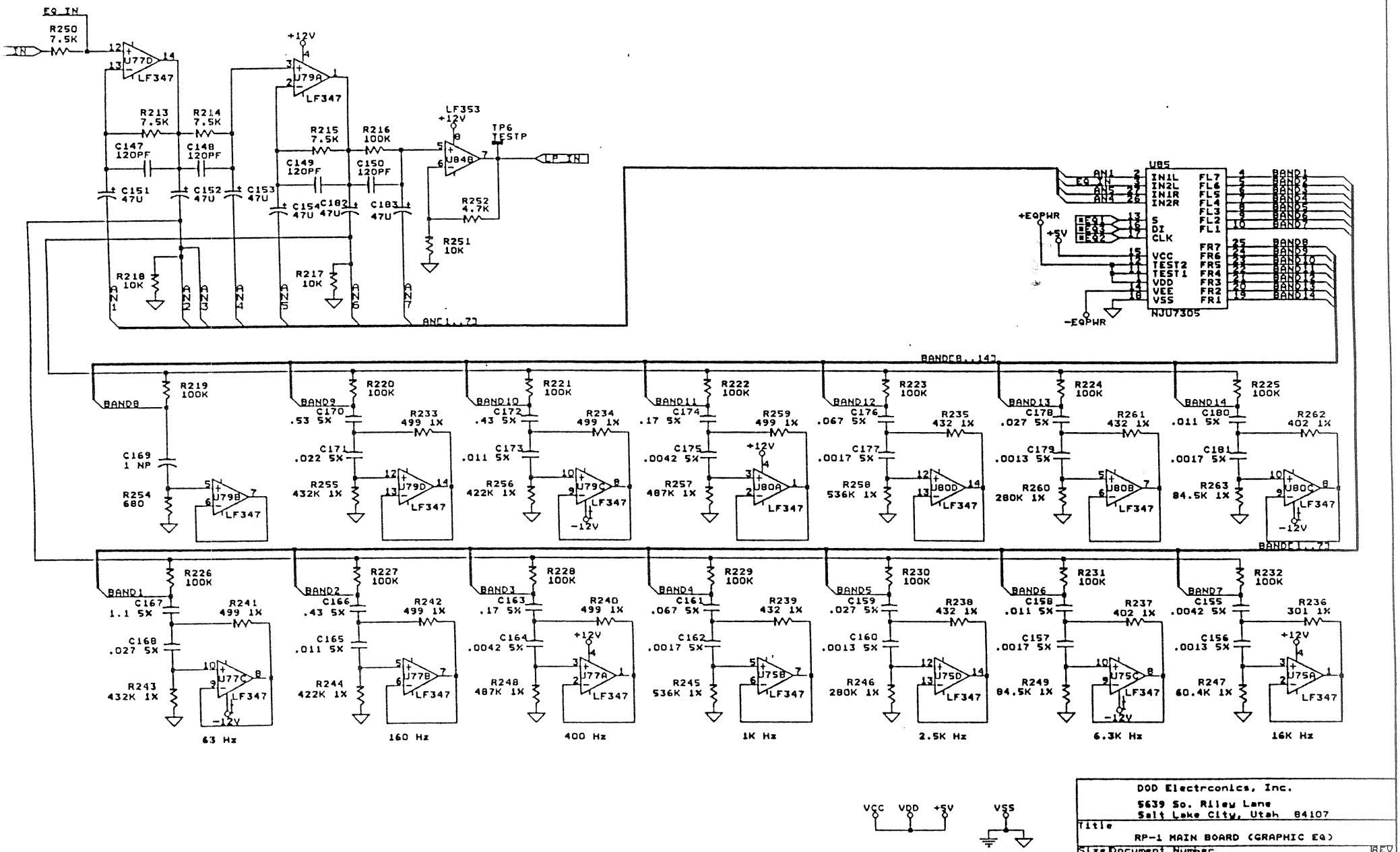

*PWRDWN
R127 100
R128 10K
R129 100K
C115 1U
R130 470K
U13A 74HC04
U13B 74HC04
U13C 74HC04
PURST
RESET
U47
74HC4040
P22
P20
X2 4.00 MHZ
C116 25PF
C117 25PF
U48
6303R
VCC
STANDBY
RESET
NMI
IRQ
XTAL
EXTAL
P10
P11
P12
P13
P14
P15
P16
P17
P20
P21
P22
P23
P24
GND
AS
R-W
E
D0-A0
D1-A1
D2-A2
D3-A3
D4-A4
D5-A5
D6-A6
D7-A7
A8
A9
A10
A11
A12
A13
A14
A15
U49A
74HC74
OVRFLO
NG_OUT
*EXT_FX_BYP
SWROW0
SWROW1
SWROW2
R131 10K
R132 10K
R133 10K
U13E 74HC04
U52A 74HC00
U52B 74HC00
U46B 74HC04
U46A 74HC04
*RD
*WR
*E
R/*W
AFD..15
ACD..15
U55
U22
U20
U21
U23
74HC574
*QUIEN2
XENEX
*QUIEN0
*QUIEN1
*QUIEN3
MCAFD..7
MCACD..7
MCODEF8
MCODEC8..15
MCODEFD..15
MCODECD..15
PDFD..7
PDCD..7
PAGEREG
PAFD..7
PACD..7
VCC
VDD
+5V
VSS
MIDI IN
J1
DIN 5
R18 100
R19 100
D1 1N4148
U50
6N138
R135 3.3K
R136 330
MIDI OUT
J2
DIN 5
C119 470PF
R139 2K
R20 200
R21 200
R137 10K
Q9 2N4124
U51D 74HC02
MIDI THRU
J3
DIN 5
C118 470PF
R140 2K
R22 200
R3 200
R138 10K
Q10 2N4124
U51C 74HC02
H8
*QUIEN4
*QUIEN7
*QUIEN5
*XNENO
DISPLAYEN
R/*W
HCN_16
Digitech
5639 So. Riley Lane
Salt Lake City, Utah 84107
Title
RP-1 MAIN BOARD (PROCESSOR, MIDI)
Size B
Document Number RP1MA803.SCH
REV A8
Date: May 18, 1992 Sheet 3 of 10

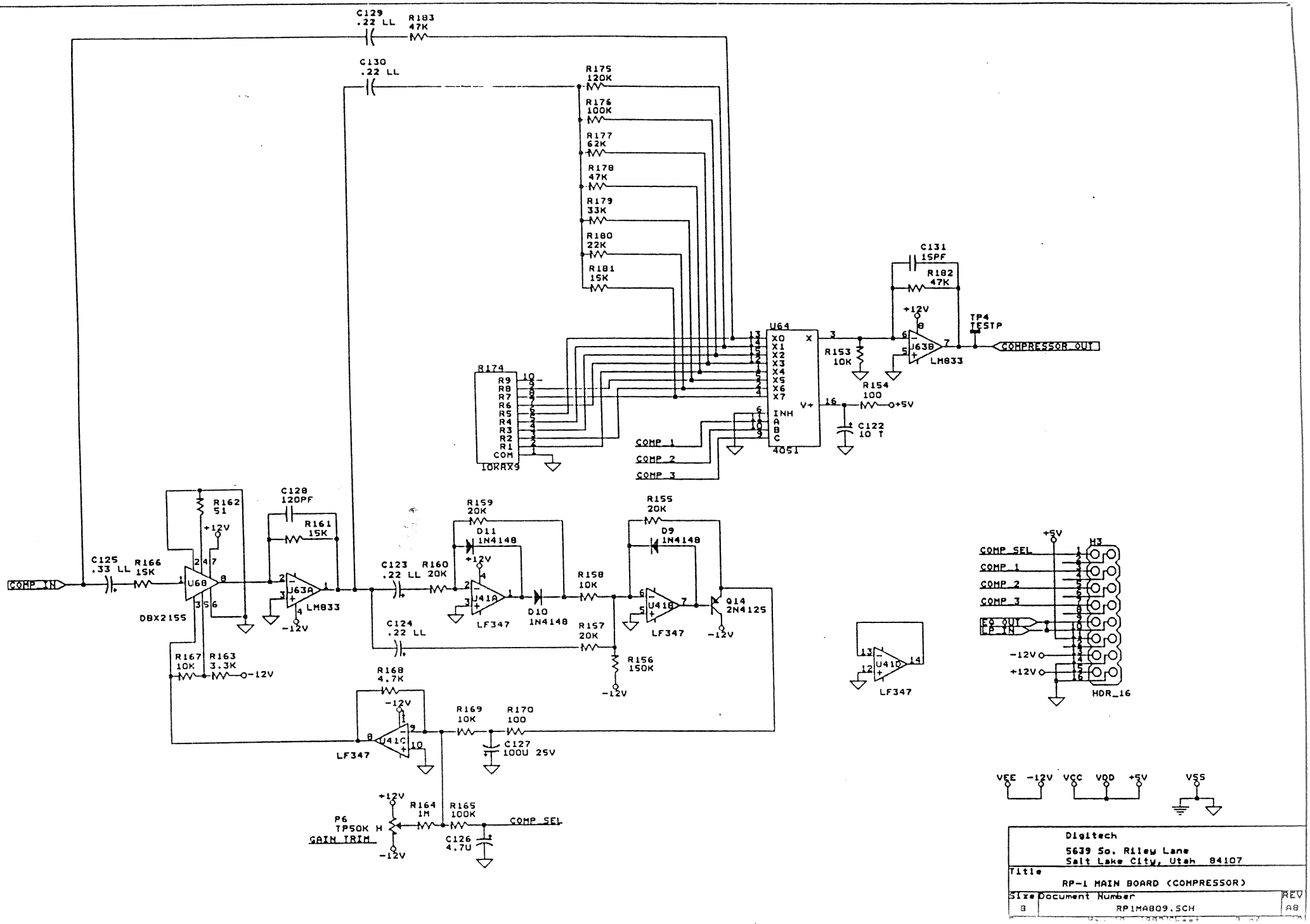

DAC0..7]
ACO..15]
U56B
74HC27
U52C
74HC00
U56A
74HC27
U57A
74HC139
U46C
74HC04
U52D
74HC00
U59
27C512-250
RP_1 V1.3
U60
6264A
U51B
74HC02
DISPLAYEN
U57B
74HC139
U51A
74HC02
U46D
74HC04
U58
74HC138
U56C
74HC27
U46E
74HC04
R31 39K
R30 20K
R29 10K
R28 4.7K
R27 39K
U5
74HC574
VPR
R144 4.7K
D8 1N4148
R145 470
D7 1N4148
Q12 2N4124
BT1 +3V CLIP
C120 4.7U
D5 1N4148
R146 1K
R147 1K
D6 1N751A
R150 4.7K
R151 10K
R152 4.7K
Q13 2N4124
Q11 2N4124
C121 15 LL
R149 1K
VCC VDD +5V VSS
Digitech
5639 So. Riley Lane
Salt Lake City, Utah 84107
Title
RP-1 MAIN BOARD (EPROM, SRAM, DECODE)
Size B
Document Number RP1MA804.SCH
REV A8
Date: May 8, 1992 Sheet 4 of 10

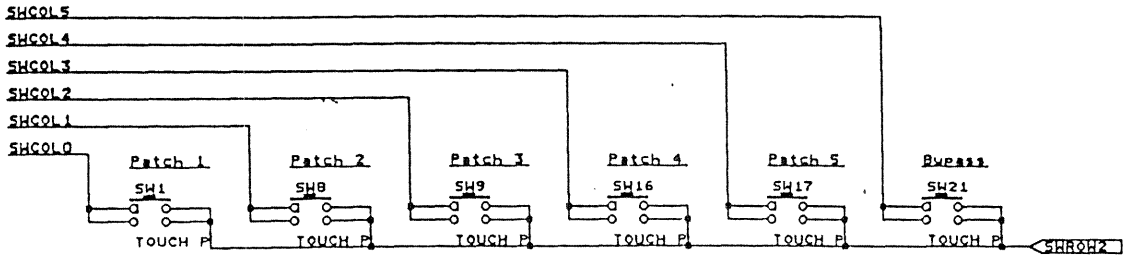

TP2 TESTP
R73 1K
R74 1K
C33 240PF
U28C
4053A
XSHL
LF353
U33A
BIAS ADJUST
P3 TP50K H
-12V +12V
R75 100K
GAIN ADJUST
P2 TP10K H
C39 15PF
U35 LM311
+12V +5V
R81 330
R83 1K
C40 240PF
R82 1K
U31C
XSHR
U36A
R85 1K
C41 240PF
R84 1K
U31A
U36B
TP3 TESTP
U34 LF357
U32 PCM54
C36 10 T
C37 BP
C34 10 T
C35 BP
C38 .010
C227 .010
R122 6.8K
R121 20K
U37A
5532
R8 10
HEADPHONES
J7 2 PH1/8 PCP
C65 BP
R120 6.8K
R119 20K
U37B
R9 10
R88 3.3K
R89 3.3K
R90 3.3K
U38D LF347
C42 .0050
C43 .018
C44 240PF
R91 3.3K
R92 3.3K
R93 3.3K
C45 .0050
C46 .018
C47 240PF
U38A
C48 10 NP
R94 10K
R95 10K
C66 .010
R96 10K
R97 1K
Q25 J112
D61 1N4148
R86 10K
U39D
P5B P20KBX216V
C49 1 NP
R4 2K
C132 120PF
R123 12K
U39A
C51 1 NP
R116 1K
RIGHT OUTPUT
J8 PH1/4 PC P
R115 470K
C52 BP
R98 10K
Q26 J112
R99 1K
D60 1N4148
D62 1N4148
R318 1M
C253 BP
R320 10K
Q29 2N4125
*ALL BYP
R319 100K
Q30 2N4124
R322 20K
R321 1M
C254 BP
R323 47K
DRY
C67 1 NP
R100 10K
R101 1K
D63 1N4148
Q27 J112
R112 10K
U39C
P5A P20KBX216V
C61 1 NP
R5 2K
C133 120PF
R124 12K
U39B
C63 1 NP
R113 1K
LEFT/MONO OUTPUT
J9 PH1/4 PC P
R118 470K
C64 BP
R102 3.3K
R103 3.3K
R104 3.3K
U38C LF347
C53 .0050
C54 .018
C55 240PF
R105 3.3K
R106 3.3K
R107 3.3K
C56 .0050
C57 .018
C58 240PF
U38B
C59 10 NP
R108 10K
R109 10K
C60 .010
R110 10K
Q28 J112
R111 1K
VCC VDD +5V
VSS
U33B LF353
DOD Electronics Inc.
5639 So. Riley Lane
Salt Lake City, Utah 84107
Title
RP-1 MAIN BOARD (A/D/A, OUTPUT)
Size B
Document Number RP1MA805.SCH
REV A8

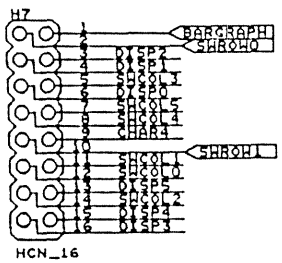

INPUT
J4
PH1/4 PC P
R38 10K
C6 .010
C5 120PF
R39 470K
U26A
LF347
+12V
R71 4.7K
R70 4.7K
C31 .56 LL
C4 8P
C7 1 NP
P1
P10K H 9V
R40 1K
C8 .22 LL
R41 10K
D2 1N4148
D3 1N4148
C9 200PF
R72 220K
U27A
LF347
C10 .22 LL
C13 25PF
R43 10K
R42 2K
U26B
LF347
C14 1 NP
R45 10K
TP1 TESTP
COMP IN
R44 10K
U26C
LF347
DRY
R46 15K
C32 240PF
R47 220K
D4 1N4148
U27D
LF347
Q8 2N4124
R330 100K
C11 1 NP
-12V
R48 10K
R331 120K
C12 .010
U27C
LF347
R63 47K
NG OUT
NG THRESH
R49 33K
R337 120K
R335 100K
R336 20K
EG OUT
U84A
LF353
FX SEND
D66 1N4148
R332 75K
D67 1N4148
R333 1M
C257 8P
Q35 J112
R334 0
EXTERNAL EFFECTS SEND
J6
PH1/4 PC P
R64 1K
C27 10 NP
C29 .33 LL
R65 15K
R68 1K
R69 470K
R87 330
C28 8P
Q31 J112
D64 1N4148
C17 25PF
R52 15K
U29B
LF347
R53 10K
R54 10K
C18 .0082
R55 10K
C19 .0012
R56 10K
U29A
LF347
R57 3.3K
C20 .0050
R58 3.3K
C21 .018
R59 3.3K
C22 240PF
U29D
LF347
R62 3.3K
C23 .0050
R60 3.3K
C24 .018
R61 3.3K
C25 240PF
U29C
LF347
AN OUT
RETURN EXTERNAL EFFECTS
J5
PH1/4 PC P
R50 10K
C26 .010
C15 120PF
R67 470K
U30B
LF353
C30 .33 LL
R66 4.7K
R51 1K
Q34 J112
D65 1N4148
C16 8P
R6 10K
Q1 2N4124
BARGRAPH
R7 470K
C50 1 LL
U30A
LF353
R324 1M
C255 8P
C256 8P
R326 10K
Q33 2N4125
R325 100K
Q32 2N4124
R328 20K
R327 1M
R329 47K
+5V
-12V
*EXT FX BYP
U27B
LF347
U26D
LF347
VCC
VDD
+5V
VSS
Digitech
5639 So. Riley Lane
Salt Lake City, Utah 84107
Title
RP-1 MAIN BOARD (INPUT, GATE, FX LOOP)
Size
B
Document Number
RP1MA806.SCH
REV
A8

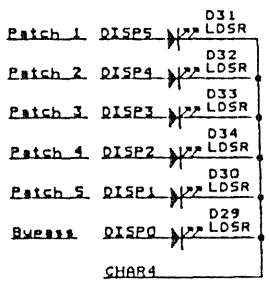

COMPRESSOR OUT
D35 1N4148
D38 1N34A
D39 1N34A
D40 1N34A
D41 1N34A
D42 1N34A
D45 1N34A
D44 1N34A
D43 1N4148
C228 .015
R267 220K
C229 .0018
D36 1N4148
D37 1N4148
D47 1N4148
D46 1N4148
R269 33K
C247 .56 LL
R297 10K
R292 10K
C239 .22 LL
R290 27K
ROCK TUBE
C248 .33 LL
R291 15K
METAL TUBE
C240 .22 LL
R281 20K
OVR DRIVE
C249 .56 LL
R282 10K
HEAVY SUSTAIN
U93
4051
R293 10K
R294 10K
R295 10K
R304 10K
C232 120PF
R299 6.8K
TP7 TESTP
U97B
LF353
R298 10K
R288 100
-12V
+5V
C238 10 T
ES IN
C250 .0082
R313 47K
R314 10K
U95A
4558
C252 1U
R317 200
Q24 J112
D59 1N4148
R315 47K
R316 10K
C251 .10
U95B
5532
C241 .047
R268 20K
U96B
5532
METAL TUBE
R283 470
Q17 J112
C245 1U
R287 10K
D58 1N4148
C243 .22 LL
R270 10K
Q20 J112
ROCK TUBE
R303 10K
R301 10K
R302 10K
R308 220K
C234 BP
R309 220K
C235 BP
D57 1N4148
R306 1M
D56 1N4148
R307 1M
C244 .22 LL
R271 10K
Q21 J112
R305 10K
R285 20K
Q22 2N4125
R286 20K
Q23 2N4124
R311 20K
R310 4.7K
R312 3.3K
C231 .0018
D48 1N4148
D49 1N4148
D50 1N4148
D51 1N4148
R279 100K
D54 1N4148
R277 470
Q18 J112
C233 1U
D55 1N4148
C230 1U
R278 470
Q19 J112
R284 10K
U91B
LM833
C246 .22 LL
R280 10K
C237 .022
D52 1N4148
D53 1N4148
R289 24K
U91B
LM833
HEAVY SUSTAIN
OVR DRIVE
U98
DBX2155
R272 51
R276 10K
C136 470PF
U96A
5532
R273 10K
R274 2K
R275 1K
C236 15 NP
C242 BP
R296 330
U97B
LF353
U92
74HC574
U94
LA10502
R300 3.3K
P7 TPSOK H
VEE -12V VCC VDD +5V VSS
DigiTech
5639 So. Riley Lane
Salt Lake City, Utah 84107
Title
RP-1 MAIN BOARD (DISTORTION)
Size B
Document Number RP1MA807.SCH
REV AB

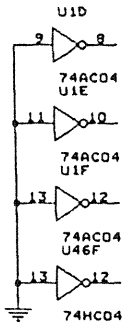

EQ IN
R250 7.5K
IN
U77D
LF347
+12V
U79A
LF347
R213 7.5K
R214 7.5K
R215 7.5K
R216 100K
LF353
+12V
TP6 TESTP
U84B
LP IN
C147 120PF
C148 120PF
C149 120PF
C150 120PF
C151 47U
C152 47U
C153 47U
C154 47U
C182
C183 47U
R252 4.7K
R251 10K
R218 10K
R217 10K
ANC1..7]
U85
AN1
EQ IN
AN3
AN4
IN1L
IN2L
IN1R
IN2R
EQ1
EQ3
EQ2
DI
CLK
VCC
TEST2
TEST1
VDD
VEE
VSS
FL7
FL6
FL5
FL4
FL3
FL2
FL1
FR7
FR6
FR5
FR4
FR3
FR2
FR1
NJU7305
+EQPWR
+5V
-EQPWR
BAND1
BAND2
BAND3
BAND4
BAND5
BAND6
BAND7
BAND8
BAND9
BAND10
BAND11
BAND12
BAND13
BAND14
BAND8..14]
BAND1..7]
R219 100K
C169 1 NP
R254 680
U79B
LF347
R220 100K
C170 .53 5%
C171 .022 5%
R255 432K 1%
R233 499 1%
U79D
LF347
R221 100K
C172 .43 5%
C173 .011 5%
R256 422K 1%
R234 499 1%
U79C
LF347
-12V
R222 100K
C174 .17 5%
C175 .0042 5%
R257 487K 1%
R259 499 1%
U80A
LF347
R223 100K
C176 .067 5%
C177 .0017 5%
R258 536K 1%
R235 432 1%
U80D
LF347
R224 100K
C178 .027 5%
C179 .0013 5%
R260 280K 1%
R261 432 1%
U80B
LF347
R225 100K
C180 .011 5%
C181 .0017 5%
R263 84.5K 1%
R262 402 1%
U80C
LF347
-12V
R226 100K
C167 1.1 5%
C168 .027 5%
R243 432K 1%
R241 499 1%
U77C
LF347
-12V
63 Hz
R227 100K
C166 .43 5%
C165 .011 5%
R244 422K 1%
R242 499 1%
U77B
LF347
160 Hz
R228 100K
C163 .17 5%
C164 .0042 5%
R248 487K 1%
R240 499 1%
U77A
LF347
400 Hz
R229 100K
C161 .067 5%
C162 .0017 5%
R245 536K 1%
R239 432 1%
U75B
LF347
1K Hz
R230 100K
C159 .027 5%
C160 .0013 5%
R246 280K 1%
R238 432 1%
U75D
LF347
2.5K Hz
R231 100K
C158 .011 5%
C157 .0017 5%
R249 84.5K 1%
R237 402 1%
U75C
LF347
-12V
6.3K Hz
R232 100K
C155 .0042 5%
C156 .0013 5%
R247 60.4K 1%
R236 301 1%
U75A
LF347
16K Hz
VCC
VDD
+5V
VSS
DOD Electronics, Inc.
5639 So. Riley Lane
Salt Lake City, Utah 84107
Title
RP-1 MAIN BOARD (GRAPHIC EQ)
Size B
Document Number
RP1MA808.SCH
REV A8
Date: May 18, 1992
Sheet 8 of 10

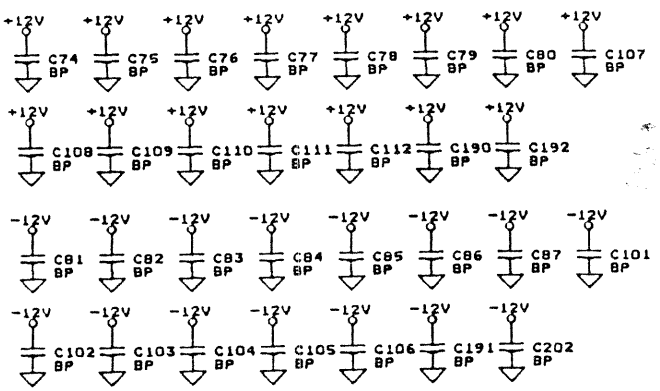

C129 .22 LL
R183 47K
C130 .22 LL
R175 120K
R176 100K
R177 62K
R178 47K
R179 33K
R180 22K
R181 15K
C131 15PF
R182 47K
+12V
TP4 TESTP
U64
X0
X1
X2
X3
X4
X5
X6
X7
INH
A
B
C
V+
4051
R153 10K
R154 100
+5V
C122 10 T
U63B
LM833
COMPRESSOR OUT
R174
R9
R8
R7
R6
R5
R4
R3
R2
R1
COM
10KRX9
COMP 1
COMP 2
COMP 3
C128 120PF
R161 15K
R162 51
C125 .33 LL
R166 15K
COMP IN
U68
DBX2155
U63A
LM833
-12V
R159 20K
D11 1N4148
C123 .22 LL
R160 20K
U41A
LF347
D10 1N4148
R158 10K
R155 20K
D9 1N4148
U41B
LF347
Q14 2N4125
C124 .22 LL
R157 20K
R156 150K
R167 10K
R163 3.3K
R168 4.7K
U41C
LF347
R169 10K
R170 100
C127 100U 25V
U41D
LF347
+5V
H3
COMP SEL
COMP 1
COMP 2
COMP 3
EQ OUT
EQ IN
-12V
+12V
HDR_16
P6
TP50K H
GAIN TRIM
R164 1M
R165 100K
C126 4.7U
VEE -12V VCC VDD +5V VSS
Digitech
5639 So. Riley Lane
Salt Lake City, Utah 84107
Title
RP-1 MAIN BOARD (COMPRESSOR)
Size B
Document Number RP1MA809.SCH
REV A8

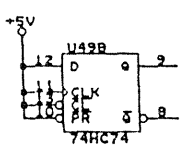


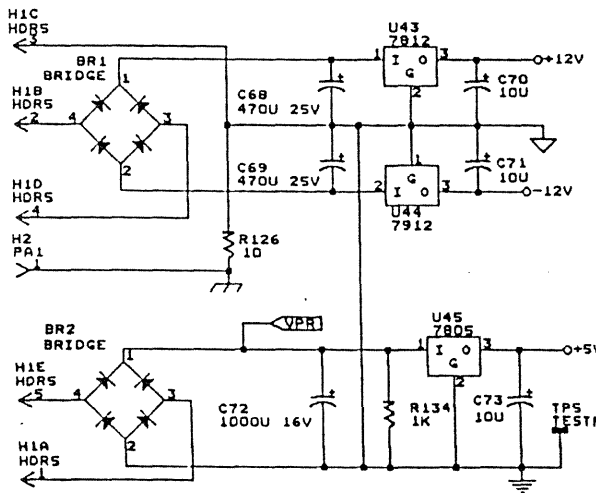


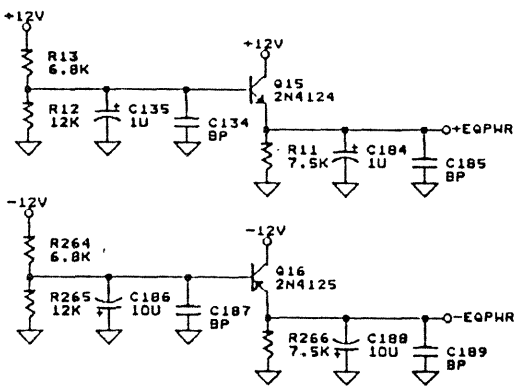


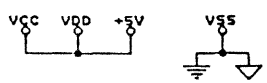


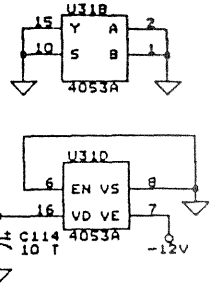






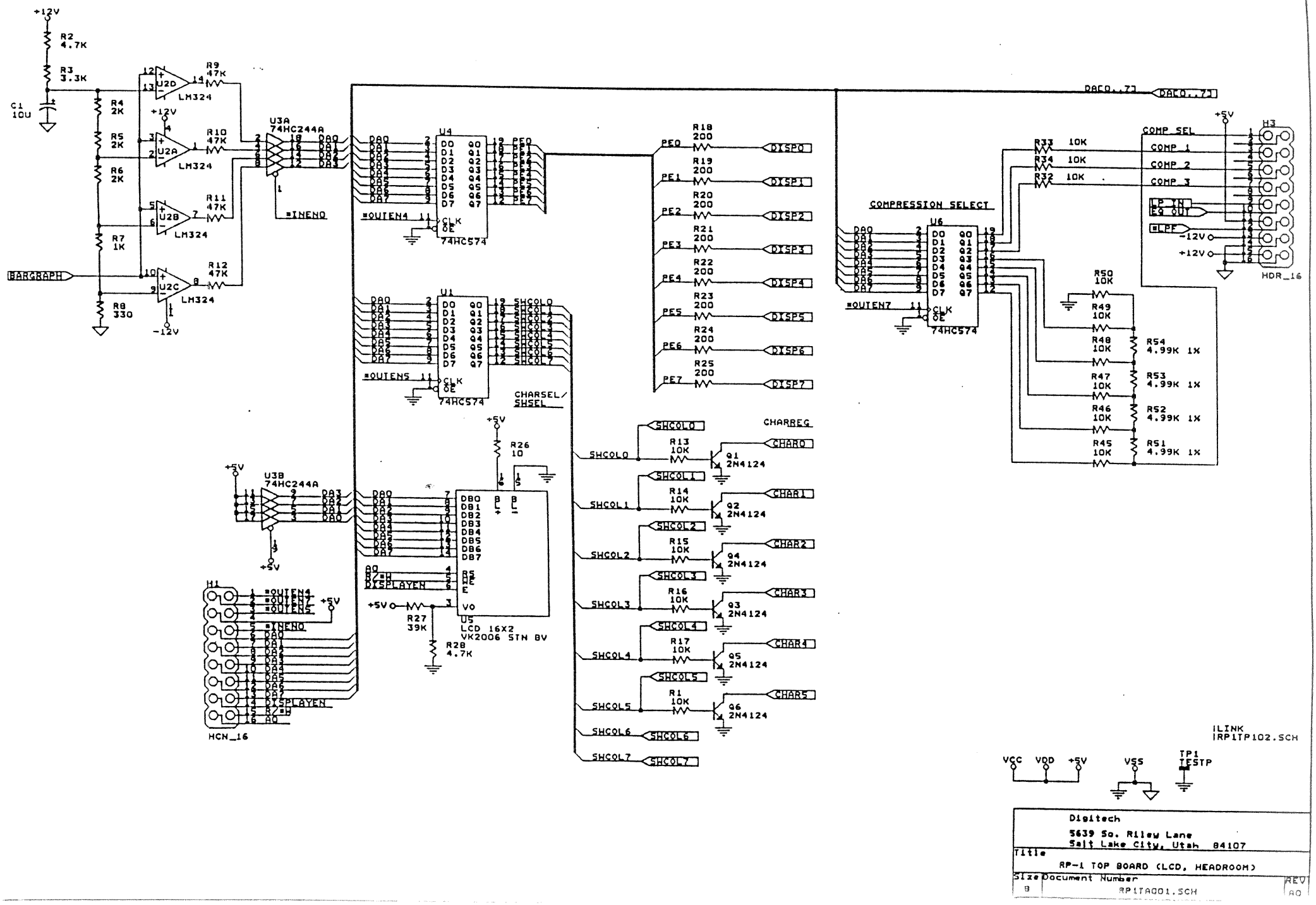


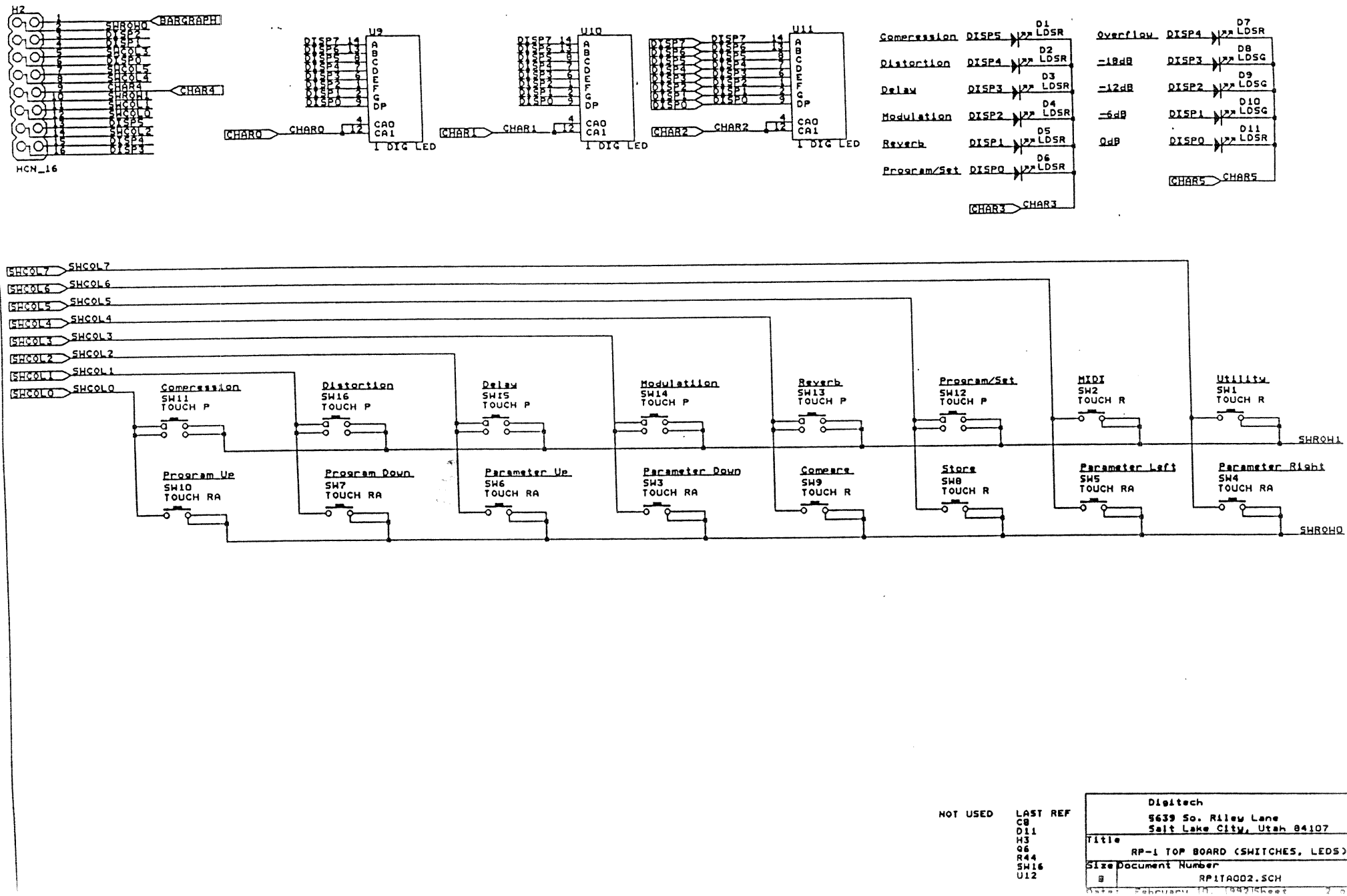




NOT USED	LAST REF.
C137-146	BR2
C192-201	BT1
C203-210	C257
D12-28	D67
H4-5	H8
P4	J10
Q3-7	P7
R14-17,23-26	Q15
R76-80	R337
R114,117	SW21
R141-143,171-173	TP7
R184-212,R253	U98
SW2-7,10-15	X1
TP5	
U17-19,24-25	
U40,42,53-54	

Digitech 5639 So. Riley Lane Salt Lake City, Utah 84107		
Title: RP-1 MAIN BOARD (POWER, SWITCHS)		
Size: B	Document Number: RP1MAB10.SCH	REV: A8
Date: May 18, 1992	Sheet 10 of 10	


+12V
R2 4.7K
R3 3.3K
C1 10U
R4 2K
R5 2K
R6 2K
R7 1K
R8 330
-12V
BARGRAPH
U2D LM324
U2A LM324
U2B LM324
U2C LM324
R9 47K
R10 47K
R11 47K
R12 47K
U3A 74HC244A
*INENO
U4
U1
74HC574
*OUTEN4
*OUTEN5
CHARSEL/ SHSEL
R18 200
R19 200
R20 200
R21 200
R22 200
R23 200
R24 200
R25 200
PE0
PE1
PE2
PE3
PE4
PE5
PE6
PE7
DISP0
DISP1
DISP2
DISP3
DISP4
DISP5
DISP6
DISP7
DAC0..7]
COMPRESSION SELECT
U6
*OUTEN7
R33 10K
R34 10K
R32 10K
COMP SEL
COMP 1
COMP 2
COMP 3
LP IN
EQ OUT
*LPF
H3
HDR_16
R50 10K
R49 10K
R48 10K
R47 10K
R46 10K
R45 10K
R54 4.99K 1%
R53 4.99K 1%
R52 4.99K 1%
R51 4.99K 1%
U3B 74HC244A
R26 10
R27 39K
R28 4.7K
U5
LCD 16X2
VK2006 STN BV
DISPLAYEN
H1
HCN_16
SHCOL0
SHCOL1
SHCOL2
SHCOL3
SHCOL4
SHCOL5
SHCOL6
SHCOL7
CHARREG
CHAR0
CHAR1
CHAR2
CHAR3
CHAR4
CHAR5
R13 10K
R14 10K
R15 10K
R16 10K
R17 10K
R1 10K
Q1 2N4124
Q2 2N4124
Q4 2N4124
Q3 2N4124
Q5 2N4124
Q6 2N4124
ILINK IRP1TP102.SCH
VCC
VDD
+5V
VSS
TP1 TESTP
Digitech
5639 So. Riley Lane
Salt Lake City, Utah 84107
Title
RP-1 TOP BOARD (LCD, HEADROOM)
Size B
Document Number RP1TA001.SCH
REV A0



NOT USED

LAST REF
C8
D11
H3
Q6
R44
SW16
U12

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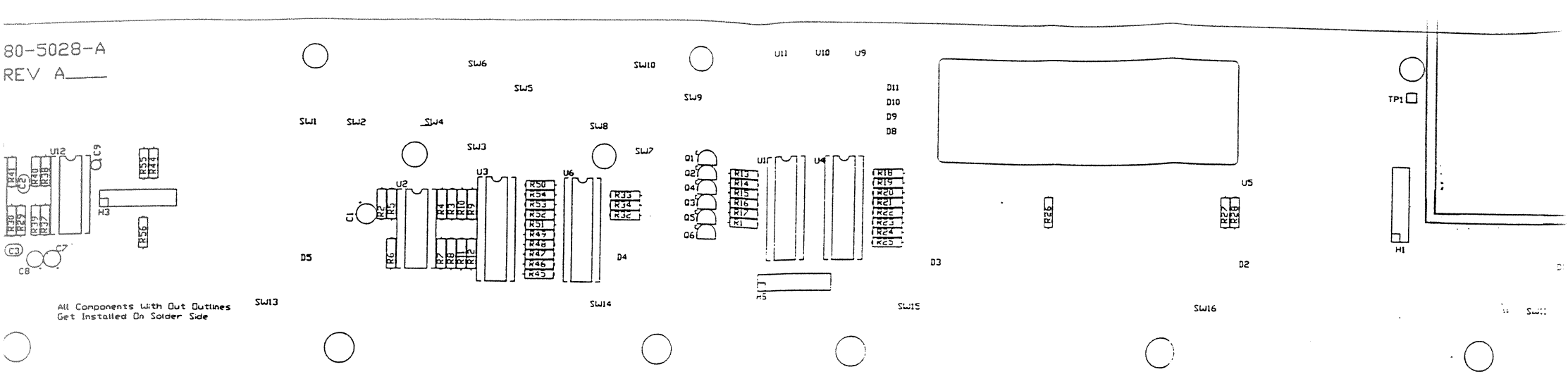
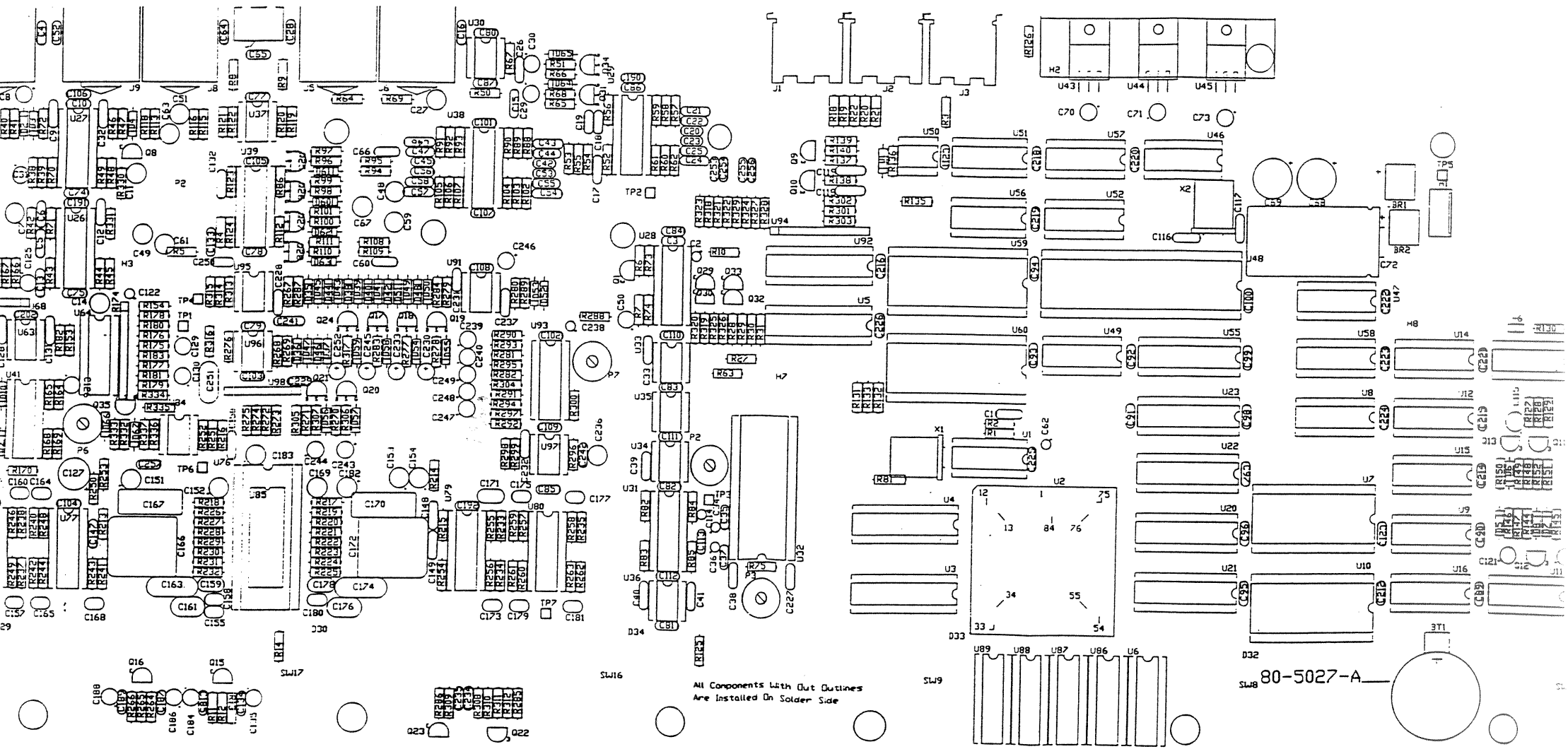
Title
RP-1 TOP BOARD (SWITCHES, LEDS)

Size	Document Number	REV
B	RP1TA002.SCH	A0

Date: February 10, 1992 Sheet 2 of


80-5028-A
REV A
All Components With Out Outlines
Get Installed On Solder Side
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
SW13
SW14
SW15
SW16
U1
U2
U3
U4
U5
U6
U9
U10
U11
U12
D1
D2
D3
D4
D5
D8
D9
D10
D11
Q1
Q2
Q3
Q4
Q5
Q6
TP1
H1
H3
C1
C2
C3
C7
C8
C9


All Components With Out Outlines
Are Installed On Solder Side
80-5027-A

VDD 1
MSREG 2
LSREG 3
D 4
*SHR 5
*SHL 6
OVRFLO 7
GATE 8
TEST 9
CLK 10
VSS 11
*12K 12
RQUD 13
*SWR 14
*ENEX 15
MCA7 16
MCA6 17
MCA5 18
MCA4 19
MCA3 20
MCA2 21
VDD 22
MCA1 23
MCA0 24
MCODE15 25
MCODE14 26
MCODE13 27
MCODE12 28
MCODE11 29
MCODE10 30
MCODE9 31
MCODE8 32
MCODE7 33
MCODE6 34
MCODE5 35
MCODE4 36
MCODE3 37
MCODE2 38
MCODE1 39
MCODE0 40
DATA0 41
VSS 42
DATA1 43
DATA2 44
DATA3 45
DATA4 46
DATA5 47
DATA6 48
DATA7 49
DATA8 50
DATA9 51
DATA10 52
VSS 53
VDD 54
DATA11 55
DATE14 56
DATA13 57
DATA12 58
DATA19 59
DATA18 60
DATA17 61
DATA16 62
DATA15 63
VSS 64
*CAS 65
*DWR 66
*RAS 67
RAMADR0 68
RAMADR1 69
RAMADR2 70
RAMADR3 71
RAMADR4 72
RAMADR5 73
RAMADR6 74
RAMADR7 75
VSS 76
DAC0 77
DAC1 78
DAC2 79
DAC3 80
DAC4 81
DAC5 82
DAC6 83
DAC7 84

FUNCTIONAL PIN DESCRIPTION FOR HISC

Description	Pin
VSS: ground (GND)	1,20,32,43,54
CLK: oscillator input	2
TEST: in-house test only (GND)	3
GATE: in-house test only (GND)	4
OVRFLO: indicates internal math overflow	5
SHL: sample/hold left	6
SHR: sample/hold right	7
D: DAC compare input	8
LSREG: clocks lower byte DAC output	9
MSREG: clocks upper byte DAC output	10
VDD: +5V power	11,42,74
DAC7..DAC0: DAC output data	12,13,14,15,16,17 18,19
RAMADR7..RAMADR0: DRAM address output	21,22,23,24,25,26 27,28
RAS: DRAM row address strobe	29
DWR: DRAM write	30
CAS: DRAM column address strobe	31
DATA19..DATA0: DRAM data	33,34,35,36,37,38, 39,40,41,44,45,46, 47,48,49,50,51,52, 53,55
MCODE0..MCODE15: microcode data	56,57,58,59,60,61, 62,63,64,65,66,67, 68,69,70,71
MCA0..MCA7: microcode address	72,73,75,76,77,78, 79,80
ENEX: enable external microcode write	81
SWR: external microcode write line	82
RQUD: request for microcode update	83
12K: in-house test only (+5V)	84